**ELECTRICAL & ELECTRONIC ENGINEERING**

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Author : **BONALA ANIL KUMAR**

Title of the thesis : **MULTI-OBJECTIVE MODEL PREDICTIVE CONTROL OF GRID-TIED SOLAR PHOTOVOLTAIC SYSTEM**

Guide : **Dr. S. SRINIVASA RAO**

Degree : **Ph. D.**

Student ID No. : **701406**

**ABSTRACT**

 Over the last few years, the largest ever increasing installed capacity of solar photovoltai (SPV) energy sources has attracted the attention of global electrical power generation market. The large penetration of grid-interactive SPV systems has enforced strict grid-codes to concern about the stable and secure operation of the existing grids. The stochastic behaviour and the strict grid-codes of SPV systems necessitate power electronic based energy conversion systems. Further, increase in the power levels of SPV systems enjoins the need for multi-level inverters and their control techniques. Multi-level inverters are well proven technology for efficient energy conversion in high power industrial applications. Neutral point clamped (NPC) topology is one of the most widely used and commercially accepted multi-level inverters of grid-tied SPV systems. Control schemes for these grid-tied NPC inverters are crucial for efficient energy conversion. The design and development of new control schemes for the grid-tied SPV inverters is an ongoing research topic.

 The major control requirements of a general grid-tied inverter includes an ideal current/power tracking, fast dynamic response, better utilization of DC-link voltage, lower current THD, and lower switching losses. However, in addition to these the specific objectives of grid-tied three-level NPC (3L-NPC) PV inverters include maximum power extraction, DC-link capacitor voltage balancing and leakage current reduction etc. Several classical control schemes are available in the literature, out of which voltage oriented control (VOC) with space vector modulation (SVM) and direct power control (DPC) based on lookup-table (LUT) approach are the most widely used control schemes of the SPV system. However, due to the complexity in the design procedure for these control schemes to include multiple objectives of SPV system has motivated the investigation of advanced control schemes.

 Finite control set model predictive control (FCS-MPC) is a class of predictive control approach which have emerged recently for the applications of power converters and energy conversion systems. FCS-MPC refers to a controller that explicitly uses the discrete-time model of the system to directly generate the switching state required for the converter defined with various constraints. The control variables required for the desired objectives are modeled in terms of the inverter switching states and the future behaviour of these variables are predicted by using the number of admissible switching states of the inverter.

 An objective function is formulated by using these predicted values and corresponding reference value. A suitable control action for the inverter is selected by minimising the objective function. However, inclusion of diverse control parameters like inverter current/power, DClink voltage, leakage current/common-mode voltage (CMV), and switching frequency into single objective function requires a suitable selection of weighting factors to maintain the relative importance between them. Usually, empirical method is used for the selection of weighting factors, which is a heuristic process and requires more number of simulation and experimental trials. This method becomes more complex and further time-consuming with the increase in number of control objectives. Selection of weighting factors is one of the challenging tasks in the design of FCS-MPC technique. Despite of multi-objective control capability, FCS-MPC still includes a classical proportional-integral (PI) controller for the DC-link voltage regulation of single-stage grid-tied SPV inverter. The outer DC-link voltage has to be regulated to its reference obtained from the MPPT algorithm to extract the maximum power from the PV array. This DC-link voltage control loop is in cascade with the inner predictive current/power control loop. Hence, the dynamics of this DC-link voltage controller influences the overall system performance.

 In this research work, efforts are made to address these limitations by introducing simplified methods for weighting factor selection with a centralized model predictive control (CMPC) approach. A simple direct optimization method and two dynamic objective prioritisation approaches of MCDM methods are proposed to simplify the selection of weighting factors. The proposed techniques presented are: selective FS-MPC under direct optimisation, CRITIC and PSI based objective prioritisation approaches under MCDM methods. Further, CMPC with decoupled active-reactive power control is proposed for regulating the floating DC-link of single-stage grid-tied SPV inverter for eliminating the cascaded structure of the FCS-MPC. All the proposed techniques eliminate the heuristic offline selection of weighting factors. The simulation model for single-stage grid tied 3LNPC PV inverter is developed by using MATLAB/Simulink to test both the classical and proposed control techniques under various operating conditions. The results are validated experimentally by using test setup developed in the laboratory. Based on the results obtained, it is observed that the proposed techniques offer an improved objective tracking and comparative dynamic response with respect to the classical approaches.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **HAREESHMYNENI**

Title of the thesis : **POWERQUALITYENHANCEMENTBY DSTATCOMWITHIMPROVEDPERFORMANCE**

Guide : **Dr. G. SIVAKUMAR**

Degree : **Ph. D.**

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**ABSTRACT**

 In present day, major power consumption loads on distribution system have been reactive in nature, such as fans, pumps, motor drives and power electronic converters. The excessive reactive power consumption results of low power factor and poor voltage reg- ulation and which reduces the active power flow capability in the distribution system. Moreover, the proliferation of power electronic devices in the distribution system worsens the operating conditions and leads to power quality problems. The major power quality issues in the three-phase distribution system are current harmonics, voltage harmonics, reactive power consumption, load unbalancing and excessive neutral current. Harmonic regulation guidelines such as IEEE 519-1992 and IEC 61000 are applied to limit the current and voltage harmonic levels. To satisfy these guidelines, the harmonics must be mitigated by using harmonic filters. Passive and active filters are used either together to form hybrid filters or on an individual basis to mitigate harmonics. In re-cent years, with the advent of sophisticated electrical and electronic equipment, Power Quality (PQ) has become an issue of concern and extensive research is being done to improve power quality.

 A promising group of solutions that deals with power quality problems in the distribu- tion system are Custom Power Devices (CPDs). The family of CPDs includes Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR) and Unified Power Quality Conditioner (UPQC) which are used for compensating power quality problems. Among these members, DSTATCOM is a shunt connected device, which mitigates current related power quality problems. In this thesis, an attempt has been made to develop a split-capacitor DSTATCOM for power quality improvement in three-phase four-wire (3P4W) distribution system. It is well known that high performance and cost-effective converter are a prerequisitefor the realization of DSTATCOM. These converters can be broadly categorized into two classes, namely, Voltage Source Converter (VSC) and Current Source Converter (CSC). The discussion about the performance of the VSC and CSC as a power circuit of DSTATCOM is beyond the scope of this thesis. In the present work, VSC has been considered as a power circuit for DSTATCOM as it has higher market penetration and more noticeable development over the last decades, in comparison to CSC topologies. In the present work, DSTATCOM has been used to mitigate harmonics, reactive power compensation and balancing of three-phase source currents. A new methodology is proposed to improve the performance of DSTATCOM with more appropriate design of dc-link voltage. For that, a reference dc-link voltage is derived based on the load operating point. With this approach, the switch voltage stress and switching losses are reduced when compared to conventional fixed dc-link voltage method. The switching losses in the proposed method are calculated and are compared with conventional fixed dc-link voltage method. The proposed variable dc-link voltage method is validated by simulation and experimental studies.

 An attempt has been made to reduce the required value of interfacing inductance in DSTATCOM applications, since it makes the system bulky and expensive. For that an LCL-filter based DSTATCOM is implemented based on switching dynamics, which improves DSTATCOM performance. In addition to current control, the application of LCL-DSTATCOM has been extended to voltage control intended for voltage regulation at PCC. The proposed method is validated by simulation and experimental studies. The method which is available in the literature to reduce the rating of VSC is a LC-filter based DSTATCOM topology. In which, an ac-capacitor is connected in series with the interfacing inductor. The series ac-capacitor supports the inverter voltage such that the dc-link voltage requirement is reduced. The amount of dc-link voltage required depends on series ac-capacitor voltage, which indeed depends on the current flowing through the capacitor. In existing methods, the dc-link voltage is fixed even through ac-capacitor voltage is varied, which leads to more voltage drop across interfacing inductor, results in degrading the performance of DSTATCOM. A new methodology is proposed, in which the dc-link voltage requirement corresponding to ac-capacitor voltage support is calculated and it has been maintained, such that the performance is improved

 An attempt has been made to integrate Solar Photo-voltaic (SPV) to grid by DSTATCOM. In general, the SPV is integrated with grid through a DC-DC converter and VSC, which is named as two-stage conversion. In view of efficiency of system, the single-stage conversion becomes more popular and in which Maximum Power Point Tracking (MPPT) of SPV and real power injection are achieved with VSC alone. But, if single-stage conversion system consists of Battery Energy Storage (BES) on dc-side of VSC, then to achieve simultaneous operation of MPPT and real power injection, a co-ordination control is required. In the proposed single-stage grid connected SPV and BES system a co-ordinate control is implemented along with energy management. In this method, the algorithm coordinates VSC and BES system based on the State of Charge (SoC) of the battery and available SPV power so that MPPT and power injection are achieved simultaneously. The proposed method not only injects real power, but also compensates reactive power and mitigate harmonics. Further, an active rectification operation during non-SPV hours is achieved. The multi-functional features of the proposed method are explained using simulation studies and are also validated through experimental studies.

**KEYWORDS:** Distribution Static Compensator (DSTATCOM); distribution system energy management; harmonics; LCL-filter; power quality; reactive power; solar photo-voltaic; switching losses; voltage source converter; voltage stress.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **HARI PRIYA VEMUGANTI**

Title of the thesis : **REDUCED SWITCH COUNT MULTILEVEL INVERTERS: TOPOLOGIES, PWM SCHEMES AND FAULT TOLERENT OPERATION**

Guide : **Dr. D. SREENIVASA RAO**

Degree : **Ph. D**

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**ABSTRACT**

 The fast growing energy needs and drastic globalization have increased the requirement of reliable, high efficient and uninterruptible power for various industrial, transport, telecommunication, aerospace, traction, energy storage, residential and domestic applications. Hence, an efficient and controllable power converter is a pre-requisite for meeting the desired specifications at the load end. Conventional controllers such as thyratrons, mercury-arc rectifiers, magnetic amplifiers and rheostat controllers possess various limitations in terms of size, cost, complexity, maintenance, reliability, efficiency, safety and robustness. The advent of self-commutating devices, the era of power converters have changed enormously. Among, ac-dc (rectifiers) and dc-ac (inverters) converters plays a significant role in most of the applications.

 AC-DC power conversion can be broadly categorised into voltage source (VSI) and current source inverters (CSI). However, one may prefer CSI due to its robustness or the VSI due to its high efficiency, low initial cost, and smaller physical size. Among these, VSI based power converters has been considered in the present work as they have higher market penetration and noticeable development in last two decades. The poor harmonic performance, high device ratings and requirement of input and output filters makes the two-level VSI impractical for direct use in high-power, medium-voltage applications. Thus, to realize VSI for high-power applications, multi pulse and multilevel inverters (MLI) are the two popular solutions reported in literature. The first one requires phase-shifting transformers which increases the converter size, cost and complexity. However, the later one does not involve any phase-shifting transformers and can be directly incorporated for high-power medium-voltage applications with matured medium power electronic devices. Owing to this, MLIs have gathered much attention in industry and academia as one of the preferred choice for high-power applications and successfully made their way into the industry.

 MLIs are proven as a matured technology for various commercialized and customized products for a wide power range of applications such as traction, compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, electric vehicles, reactive power compensators, renewable energy generation, custom power devices, marine propulsion, high-voltage direct-current (HVDC) transmission. Among the topologies of MLIs, diode clamped (DCMLI), flying capacitor (FCMLI), and cascade H-bridge (CHB) are widely popular and termed as classical MLIs. These topologies gathered a great attention both from academia and industry. Their practical implementation is heavily influenced by the application, control complexity and cost. The requirement of large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low power rating applications. The requirement of large number of capacitors and their pre-charge requirement limits FCMLI to high bandwidth applications such as traction drives.

 The modular structure and high fault tolerance ability makes CHB best suited for high-voltage medium-power applications (13.8 kV, 30 MVA). However, CHB requires isolated dc sources for active power transfer applications. As similar to DCMLI and FCMLI, switch count of CHB increases with number of levels in phase-voltage. In addition, topologies of classical MLIs present great deal of challenge in implementation to higher levels. This is due to its increased device count at higher levels, which complicates its circuit configuration and imparts size, cost and maintenance limitations. Hence, researchers continued to explore and evolve newer topologies by making more or less changes on the classical MLIs. CHB with unequal dc link voltages or hybrid combination with DCMLI can increase the number of levels with significant reduction in switch count. However, unequal blocking voltages of switching devices and limited switching redundancies of these topologies cause uneven utilization of dc sources.

 The increased component count of power semiconductor devices and capacitor/dc sources of classical MLI topologies has provoked the researchers to contribute further to evolve newer topologies with reduction in size and cost. Thus, MLI with reduced device count originated and this domain of MLIs are called as reduced switch count (RSC) MLIs. From the past decade, various enthusiasts carried out extreme research on RSC-MLIs and developed numerous topologies with significant reduction in component count, total blocking voltage, cost and ease of control. Several RSC-MLI topologies such as multilevel dc link (MLDCL), packed U-cell (PUC), cascaded bi-polar switched cells (CBSC), reverse voltage (RV), switched dc sources (SDS), basic unit MLI, envelope-type (E-type), T-type, hybrid T-type, series-connected switched sources (SCSS), switched series parallel sources (SSPS), nested MLI, switched capacitor unit, reduced cascaded and various other three-phase and cascaded topologies are reported in literature.

 In this connection, qualitative and quantitative features of RSC-MLI topologies have discussed in this thesis and, a comparison has made to facilitate a well-informed selection of topology for a given application. For this, a comprehensive comparison between various RSC-MLI topologies is presented in terms of performance parameters such as device count, device ratings, blocking voltages, requirement of bi-directional switches, nature of dc link, modularity, fault tolerant ability, switching and conduction losses, power distribution and utilization of dc link voltages. Considering the above factors, RSC-MLIs are categorized into symmetrical and asymmetrical configurations, topologies with separate level and polarity generator, generalized and unit-based configurations, H-bridge and hexagonal switch cell (HSC) structures, topologies with unidirectional and bi-directional switches, topologies with isolated/floating dc sources and topologies with series/parallel operation of dc sources.

 The reduction in switch count, even power sharing among dc voltage sources and adequate switching redundancies are the paramount criteria for the selection of inverter topology. Among these, MLDCL possess simplified and modular structure with appreciable reduction in switch count, multiple switching redundancies, symmetric and simplified switching operation, fault tolerant ability, even power distribution, equal device blocking voltages and dc link voltage balancing ability. Owing to these key and worthy benefits, this topology had gathered more attention and further served as a viable alternative for CHB in applications such as grid-connected photo-voltaic system, uninterrupted power supplies (UPS), custom power devices (CPD), adjustable speed drives (ASD), battery energy storage systems (BESS), active front-end (AFE) applications and electric vehicles (EV).

 The significant reduction in switch count of RSC-MLI topologies has simplified their circuit configuration such that, each switch may involve in attaining more than one voltage level. Asymmetrical RSC-MLIs further reduced the switch count and made the topologies much simpler. However, significant reduction in switch count have reduced the redundancies and modified the switching combination such that, devices conducting for obtaining lower voltage level may not remain in conduction at higher levels as well. This acted as a limitation of conventional carrier based pulse width modulation (PWM) schemes such as level-shifted (LSPWM) and phase-shifted (PSPWM) to control these RSC-MLIs.

To control any RSC-MLI, selective harmonic elimination (SHE) and space vector (SV) PWM are often preferred. However, these schemes require elusive calculations and complexity increases at higher number of levels. Hybrid PWM is another popular scheme reported for implementing asymmetrical cascaded configurations such as CHB and SSPS (with an addition of H-Bridge). However, requires estimation of output voltage of the higher voltage bridge/units, to derive the reference signal for lower voltage bridge/units. Switching schemes using low frequency carrier reported for MLDCL, CBSC, basic unit RSC-MLI, T-type and Hybrid T-type topologies are easy to realize but, produces lower order harmonics. On the other hand, among the carrier based PWM schemes, multi reference, reduced carrier and hybrid switching function are widely popular. Multi reference modulation results high THD in line-voltage and requires multiple dc off shifted references which increases the complexity in closed loop-applications. Hybrid switching function PWM results in satisfactory THD but requires numerous comparators at higher levels, which increases computational burden. Reduced carrier PWM scheme with logical expressions are the simplest. However, these logical expressions are not generalized and vary with topology and number of levels.

 Therefore, to overcome the limitations of conventional PWM schemes of RSC-MLI, modified carrier and modulating signal arrangements are proposed in this thesis. The performance of the modified PWM schemes with the proposed carrier arrangement is evaluated on five-level inverter topologies and its superior THD performance over the conventional schemes is validated. Further, a simple carrier based PWM scheme with unified logical expressions is proposed. The proposed logical expression remains valid to control any RSC-MLI, irrespective to the voltage ratios and topological arrangement and produces good THD performance with less computation burden.

 To validate the ability of the proposed switching logic, the PWM scheme is implemented in MATLAB/Simulink environment for thirteen-level asymmetrical RSC-MLI configurations such as MLDCL, SDS, Cascaded T-type, Improved T-type and E-type. The simulation results are validated experimentally by developing various topologies of RSC-MLIs by interconnecting two inverter modules with 24 isolated IGBTs on each. The PWM scheme is implemented on d SPACE Micro Lab Box R&D controller. Further to validate the superiority of the proposed PWM scheme, its performance in-terms of computation burden and line-voltage THD is compared with the state-of-the-art PWM schemes reported in the literature.

 Another aspect for selection of inverter is its reliability. The ability of an inverter to work under fault conditions plays a vital in ensuring the safety and uninterrupted operation of the overall system. There are several reasons for occurrence of fault in inverters, and every fault will ends up with either open-circuit (OC) or short-circuit (SC) of a particular switch or associated unit/bridge. SC fault results in dangerously high current and cause a possible damage to the inverter. To avoid these faults, a fast acting over-current protection circuits are required to by-pass the faulty phase-leg or inverter. On the other hand, OC faults are not severe and can be compensable. Hence, this thesis analyses the affects and compensation of OC faults.

 The reduction in switch count of RSC-MLI has reduced the probability of fault occurrence as compared to MLI. However, the extreme reduction in switching redundancies restricted their fault tolerant ability. In literature, SVM and carrier based schemes are reported for compensating single switch fault in RSC-MLI such as T-type. Among these, SVM is an attractive scheme which can achieve fault tolerant operation (FTO) by creating switching redundancies. Nevertheless, its complex implementation acts as a limitation at higher level. In general, the fault tolerant schemes (FTS) generates a new set of modulating signals to reconfigure the inverter to achieve FTO. This FTO is feasible for modular and redundant topologies such as MLDCL.

 By-passing method is one of the most feasible FTS to restore balanced operation. However, this method of fault compensation derates the inverter as the healthy units are by-passed. To obtain FTO without derating the inverter, the burden of faulty units of one phase is shared across the healthy units of same phase such that its overall phase-voltage is equal to pre-fault voltage. This method results in non-uniform burdening of healthy units, which effects their dc link voltages and power distribution among operating units. To obtain balanced operation with equal power distribution among the healthy units, neutral shifting (NS) FTS is reported. This scheme modifies the magnitude and angle between phase-voltages such that the inverter produce balanced line-voltages with uniform burden on all healthy units. NS involves manual calculation of modified phase-angles to ensure magnitude and angle balance among line-voltages. This method can compensate multiple switch faults, only if the number of faulty units in any two phases are same. Another approach to achieve NS is to inject a zero-sequence voltage to shift the neutral point of the inverter. The magnitude of injected zero-sequence voltage depends on the number of faulty units. In literature, this method is reported on CHB for compensating single switch fault (per phase), and is not reported for compensating multiple OC faults. Moreover, this scheme is not directly applicable for tolerating OC faults on RSC-MLIs.

 Therefore in this thesis, a generalized NS zero-sequence injection FTS is proposed for compensating multiple OC switch faults on MLDCL inverter. Generalised equations are proposed to determine the magnitude of injected zero-sequence voltage and fault tolerant modulating signals, for any fault case. The proposed generalized fault tolerant modulating signals are operated with carrier rotation based reduced carrier PWM scheme to obtain balanced set of line-voltages with uniform power distribution among all the operating units. To investigate the ability of the proposed generalized FTS, simulation study on three-phase fifteen-level MLDCL inverter is performed. The inverter is controlled with the proposed modified reduced carrier PWM scheme and to achieve uniform burden among healthy operating units, the carriers are rotated at the end of each carrier time period. After the initiation of FTO, the balanced operation of the inverter is observed from their line-voltage and current waveforms and their respective RMS values. In addition, power delivered by each unit ensures the uniform performance (power distribution) among all the operating units. To corroborate the simulation results, a nine-level three-phase IGBT based MLDCL inverter is developed and controlled, using OPAL-RT 4500. However, performance of proposed FTS is validated assuming stiff sources in the dc link and the effect of charging and discharging currents on dc link voltages during fault compensation is excluded.

 Therefore, to investigate the efficacy of proposed FTS in closed-loop application, an active rectifiers is considered. Multilevel converter (MLC) based active rectifiers gained more prominence for high-power applications such as UPS, grid-connected applications, BESS, battery chargers and ASD. Owing to challenges such as voltage balance of dc link capacitors, even power sharing and fault tolerant operation, the implementation of RSC-MLI topologies as an active rectifiers is not yet reported.

 In literature, various voltage and current control techniques are reported for three-phase regenerative active rectifiers. Among these, direct power control (DPC) and voltage oriented control (VOC) are commonly used control schemes. DPC produces fast and accurate response, and involves either hysteresis, predictive or adaptive controllers, followed by PWM or look-up tables. Practice of predictive or adaptive controllers increases the difficulty in realizing DPC for MLCs/RSC-MLCs based active rectifiers. On the other hand, VOC is simple and more robust, and can be easily implemented for MLCs and RSC-MLCs. The objective behind VOC is to regulate the dc link voltages, irrespective to the load variations. On the other hand, to regulate the power delivered by the converter, irrespective to the load conditions, grid active reactive power control (GARPC) is reported. This method senses and controls the dc link voltage such that a rated power with unity power factor is delivered to the converter for any load condition. GARPC is also known as instantaneous active and reactive power control.

 The above control algorithms can be effective only if the converter is able to provide an appropriate path for charging and discharging of dc link capacitors. If the converter operation is faulty, then its operation is restricted and results dc link voltage unbalance. As the design and control of RSC-MLC based active rectifier for healthy and faulty operation of the converter is not yet reported, and therefore an attempt is made in this thesis.

 In this thesis, a three-phase, 1 MVA, 3.3 kV, fifteen-level MLDCL based active rectifier is proposed with a comprehensive control scheme. In this scheme, the control objective are achieved by involving modified reduced carrier rotation PWM and proposed fault tolerant scheme with VOC or GARPC algorithms. The pre and post-fault performance of considered MLDCL based active rectifier for dynamic variation in load, change in set-point references and regeneration operation is demonstrated in MATLAB/Simulink environment for VOC and GARPC algorithms under various fault conditions. Further, the efficacy of the proposed scheme in balancing converter dc link voltages, even power distribution of dc sources, and fault tolerant ability is demonstrated on OPAL-RT 4500 real-time controller.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **CH KASI RAMAKRISHNAREDDY**

Title of the thesis : **SOFT-SWITCHED DC-DC CONVERTER CONFIGURATIONS FOR LED LIGHTING APPLICATIONS**

Guide : **Dr. S. PORPANDISELVI**

Degree : **Ph. D.**

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**ABSTRACT**

 Globally, about 19 % of total electrical energy produced is used for lighting applications. Hence lighting loads have significant potential for improving energy efficiency and cost savings. In view of this, energy efficient lighting sources need to be developed. The light emitting diode (LED) is becoming a promising lighting source over conventional lighting sources for a future generation due to its various advantages such as high luminous efficacy, long life, solid state characteristic, compactness, ease of controllability and eco-friendliness etc.

 LED lighting systems require constant current regulators to produce constant illumination. These regulators must provide the features such as high efficiency, LED load current regulation, dimming control, compact size, high reliability etc. Despite the availability of several converter configurations and control techniques, there is enough scope for further research in making a compact LED power driver with reduced component count, high efficiency and dimming control to suit various application needs. This thesis work focuses on soft-switched DC-DC converters for LED lighting applications.

 This thesis proposes four LED driver circuit configurations. The objectives are to provide high power conversion efficiency, reduced device current, powering of multiple lighting loads with dimming, zero-voltage switching, reduced size of reactive elements, driving LED lamps of different power ratings, regulation of LED lamp current against input voltage variations and configurations suitable for high power lighting application.

 The first proposed converter configuration comprises of a full-bridge topology with soft switching inductor. It is powering four LED lamps of same rating. Regulation of LED lamp current against input voltage variations is achieved using a buck-boost topology at the input side. This configuration also provides PWM dimming control of all the LED lamps. It offers zero voltage switching in devices of the bridge circuit. In this configuration, switches of the bridge circuit carry a small current which is almost independent of LED lamp currents. Hence conduction losses are reduced. This configuration provides high efficiency at both full illumination and during dimming operation. It provides an efficiency 93.88% at full illumination level. This configuration also provides reduced components count per lamp and hence reduction in cost. This configuration can be extended to multiple LED lamps by addition of legs in bridge. This configuration is suitable for street lighting as well as domestic lighting applications.

 The second proposed converter configuration consists of a full bridge topology with multi-phasing technique for ripple free current. It powers two LED lamps of same rating. It provides ripple free currents through two LED lamps. In this configuration, power processed through bridge circuit is less and hence the losses are reduced. This configuration provides current cancellation, which reduces current stress of the devices. This further reduces the conduction losses. Zero-voltage switching is obtained in bridge circuit devices. This configuration provides high efficiency at both full illumination and during dimming operation. It provides an efficiency of 94.26% at full illumination level. This configuration can be extended to multiple LED lamps by addition of legs in bridge. This configuration is suitable for street lighting as well as domestic lighting applications. This configuration allows use of small value of inductor and hence reduces size and cost. This configuration also provides PWM dimming operation and regulation of LED lamp current.

 The third proposed converter configuration consists of a three leg resonant converter. This configuration is powering two LED lamps of different power ratings. In this configuration, two series resonant circuits with different resonant frequencies are used to power two LED lamps. This circuit operates simultaneously at two different frequencies. This configuration provides regulation of LED lamp currents and independent PWM dimming control of LED lamps. It also provides ZVS operation. This configuration provides high efficiency at both full illumination and during dimming operation (>91%).

 The fourth proposed converter configuration consists of a full bridge resonant converter. This configuration is powering single LED lamp of high power rating. In this configuration, LED lamp is powered by two voltages of different magnitudes derived from series resonant converter. In this configuration, only small controlled power is used for regulating the lamp current which increases the efficiency. This configuration provides ZVS operation and PWM dimming control. This configuration provides high efficiency at both full illumination and during dimming operation (>92%). This topology is suitable for applications where lamp voltages are smaller than supply voltages like dc micro grid applications.

 All the above four proposed LED driver configurations provide LED current regulation, low or zero ripple in LED lamp currents, PWM dimming control, ZVS operation and high efficiency. All these proposed configurations are analysed, simulated and experimentally validated.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **S. KAYALVIZHI**

Title of the thesis : **OPTIMAL PLANNING OF DISTRIBUTED GENERATIONS IN DISTRIBUTION NETWORK AND LOAD FREQUENCY CONTROL OF MICROGRID USING META-HEURISTIC ALGORITHMS**

Guide : **Dr. D. M. VINOD KUMAR**

Degree : **Ph. D.**

Student ID No. : **701340**

**ABSTRACT**

 Continuous supply of electricity is the need of the hour in developing economies, more so in a rapidly industrializing country like India. The growing demand tends to change the conventional structure of power system to increase the flexibility of the existing system that generates power in bulk and deliver the power to the load centers through transmission network. To avoid transmission congestion and to assure continuous supply to scattered loads, Distributed Generations (DG) in small scale emerged as an alternative technology. Many of the DG technology sources include renewable energy sources such as wind power, photovoltaic cells, biogas, fuel cells, etc., in order to meet the environmental constraints. These DG technologies have been adopted to meet the future loadwith improved system efficiency, reliability, security and quality of service; they however have a critical impact on the system voltage, power quality, stability, fault level and protection coordination. In spite of promising improvement in reliable power supply with less green gas emission, the implementation of active distribution networks imposes a large number of technical and regulatory issues that need to becarefully evaluated. Hence, planning the DG plays a vital role in establishment of future smart grid. It is essential to have suitable and efficient methods and models to plan an active distribution network operation, which involves many objectives and constraints. Conventional methods like analytical approaches and numeric methods have been adequately applied for DG planning in distribution network in various ways. But these methods sometimes arrive at local optimal solutions in spite oftheir computational burdens. They also lack handling multi-objective problem efficiently. Population based evolutionary algorithms have been found ideal in dealing with multi-objective DG planning. However, many such algorithms suffer from premature convergence due to limited exploration in the search space while a few algorithms have their own control parameters, which will influence

the algorithm efficacy. Thus, in this thesis, a parameter less novel multi-objective based Peer enhanced Teaching-learning based optimization (PeMOTLBO) algorithm is proposed and employed to find a set Pareto optimal solutions for planning DG in distribution system and fuzzy theory approach has been used to find the best compromising DG location and size. The pareto front obtained by the proposed PeMOTLBO has been compared with basic MultiObjective TLBO (MOTLBO) and Non-Dominated Sorting Genetic Algorithm –II (NSGAII). The comparisons show the superiority of the proposed algorithm in terms of both better objectives and diversity among the solutions in the optimal fronts obtained. Two performance metrics have been evaluated to ascertain the two goals of the multi-objective optimization and the proposed technique exhibited better metricvalue compared to NSGAII and MOTLBO. It is well known that there are several DG technologies which are costlier and polluting, such as diesel and gas, as well as environment friendly technologies such as wind and solar. Planning the optimal operation of DGs to supply the load is the ultimate requirement of Active Distribution Network (ADN) operation. In view of this, a new hybrid Grid-based Harmony Search algorithm is proposed by incorporating the grid based strategy in the basic harmony search algorithm for multi-objective DERs planning model both in grid connected and autonomous microgrid operation with three conflicting objectives viz., i) Energy loss ii) voltage deviation and iii) cost of DG integration. A qualitative comparison is also made with two comparison metrics to ascertain the superiority of the proposed algorithm over robust NSGA-II and other form of multi-objective harmony search. A grid based multi-objective harmony search optimization is proposed to find the optimal mix of DG units for economic operation of grid connected distribution system and it has been extended to analyze autonomous operation of active distribution system in the presence of battery storage. While planning the DGs and their economic feasibility for operation in micro grid, the main purpose of microgrid operation should not be ignored i.e. the active management of load that is directly linked with the approximately constant frequency of operation in the system. Thus, load frequency control of an isolated micro grid is also attempted in this thesis with two types of control techniques: first one with PI controller, whose gains are tuned with Levy-based spider monkey optimization algorithm. This method employs levy flights to explore the search space whereas spider monkey algorithm is utilized to intensify the search towards better optimal solution. And the second, a fuzzy adaptive Model Predictive Control (MPC), where the fuzzy controller is embedded into MPC algorithm for better adaptive performance of load frequency control in an isolated micro grid.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **O.V.S.R.VARAPRASAD**

Title of the thesis : **ADVANCED SIGNAL PROCESSING TECHNIQUES FOR REAL-TIME ESTIMATION AND CONTROL OF HARMONICS IN SMART ELECTRIC GRID**

Guide : **Dr. D.V.S.S. SIVA SARMA**

Degree : **Ph. D.**

Student ID No. : **701232**

**ABSTRACT**

The paradigm shift from the conventional electric grid to a smart electric grid leads to many operational challenges. The modern power electronic based nonlinear loads are causing severe harmonic pollution in the distribution system. A crucial challenge for the smart electric grid is to effectively estimate and control the harmonics in the power system, which requires precise and real-time estimation of the amplitude, phase, and frequency of the power system. The proliferation of harmonics, mainly in a distribution system produced by extensive diffusion of nonlinear loads, power electronic converters, will deteriorate the accuracy of estimation of amplitude, phase, and frequency and at the same time making it hard to track the power system voltage, current and frequency variations. The prime objective of this doctoral thesis work is to develop advanced signal processing techniques that can provide an accurate and fast estimation of all the current harmonic components and also develop selective control techniques to control the harmonics in a smart electric grid.

Consciousness to reduce harmonics in the low voltage distribution grid is increasing because these harmonics significantly affect the operation of the smart electric grid in terms of safety and economy. The methodology must be simple and allow fast computation for harmonics with retrofit computation capabilities. This research work contributes towards real-time estimation of harmonics and their compensation in a modern distribution network. Moreover, for real-time estimation and control of harmonics is essential to have fast and accurate algorithms and associated controllers.

The objective of this thesis is to develop and design methods to estimate and control current harmonics, which are introduced in the distribution system by various nonlinear loads such as consumer electronic equipment i.e. Compact Fluorescent Lamp (CFL), Light Emitting Diode (LED) bulbs, personal computers, printers, scanners, charging units and so forth. The current harmonics produced by the non-linear loads affect the performance of neighbouring linear loads and injects the same to grid which in turn impact the appliances of other innocent residential consumers who does not install harmonic compensation devices in their premises.

Chapter 1 gives the overview of current harmonics problem on smart electric grid, detailed literature survey on estimation and control of harmonics and the author’s contribution for estimation and control of current harmonics in the smart electric grid. Chapters 2 and 3 are dedicated to the estimation of current harmonics, which are periodic and also time-varying in real-time using National Instruments (NI) Compact reconfigurable input-output system (cRIO) v 9082. Chapter 4 focus on control of harmonics with Conservative power theory (CPT) based Hybrid Active power filter, Chapter 5 introduces a think-ahead decision making algorithm & CPT based three-phase multifunctional grid-connected PV inverter which minimizes the grid consumption and exploits the full benefit of solar generation simulates various cases of load conditions and validates in real-time using OPAL-RT. Chapter 6 describes the multi-band hysteresis current controlled single-phase multifunctional grid-connected PV inverter interfaced with rooftop solar PV.

The estimation methods developed in this thesis also empower utilities to introduce policies to penalize causes injecting harmonics into the grid and further encourage the introduction of control mechanisms at the same and realize “Swatch Power” (a “Pure Power” with smart features).

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **KUNISETTI V PRAVEEN KUMAR**

Title of the thesis : **INVESTIGATION OF DIRECT TORQUE CONTROL AND PREDICTIVE TORQUE CONTROL STRATEGIES TO AN OPEN-END WINDING INDUCTION MOTOR DRIVE**

Guide : **Dr. T. VINAY KUMAR**

Degree : **Ph. D.**

Student ID No. : **715021**

**ABSTRACT**

 Now-a-days, multi-level inverter (MLI) fed induction motor drives have turned as an interesting area for researchers. This thesis focuses on direct torque control (DTC) and predictive torque control (PTC) strategies for the OEWIM drive to curtail ripples in torque, flux, switching frequency and common-mode voltage (CMV). The scheme of DTC offers high dynamic performance and control algorithm in stationary reference frame. In practice DTC also has several limitations. In this thesis, an attempt is made to address some of the limitations and also to provide improved versions of DTC algorithm. If the two inverters of OEWIM are fed with equal DC-link voltages then it provides two-level and three-level inversion. By operating OEWIM drive with unequal DC-link voltages (2:1 ratio); then it gives four-level inversion. To implement three-level and four-level inversion fed DTC algorithms, a three-level torque hysteresis controller and two-level flux hysteresis controllers are used. The voltage vectors are categorized into various groups for three-level and four-level inversion. Proposed MLI fed DTC algorithms can reduce torque and flux ripples, whereas its implementation is cumbersome. In order to address these problems, fast and accurate torque control methods are needed. Fast and accurate torque control can be obtained by employing model predictive control (MPC).

 The combined features of MPC and DTC give an effective control strategy for OEWIM drives known as finite control set predictive torque control (FCS-PTC) or simply predictive torque control (PTC). In this thesis a modified cost function based PTC has been introduced to reduce CMV of OEWIM drive fed with two, three and four-level inversion. The limitation of this algorithm is that the cost function comprises of dissimilar quantities, the selection and tuning of weighting factors is unavoidable. To simplify the selection and tuning of weighting factors; normalized weighted sum model (NWSM) based PTC and weighting factor eliminated (WFE) PTC schemes are proposed for the OEWIM drive. The average switching frequency of OEWIM drive can be reduced by NWSM PTC or WFE PTC.

 The proposed DTC and PTC strategies are developed in MATLAB/SIMULINK. To verify the effectiveness of the proposed DTC and PTC strategies, these are tested experimentally. The experimental and simulation results are compared with classical DTC and PTC strategies.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **RATNA RAHUL TUPAKULA**

Title of the thesis : **INVESTIGATION ON CONTROL STRATEGIES FOR GRID AND OFF-GRID CONNECTED INVERTERS IN DISTRIBUTED GENERATION SYSTEM**

Guide : **Dr. D.M. VINOD KUMAR**

Degree : **Ph. D.**

Student ID No. : **714122**

**ABSTRACT**

Globally, with the gradual exhaustion of fossil fuels, increase in carbon emissions and global warming, the quest for renewable energy sources has gained prominence. Among renewable sources, Photo voltaics (PV) has gained importance because of its easy deployment and considerable advantages over other renewable sources like wind, tidal etc. As all the renewable energy sources are intermittent in nature, it will be a noble idea if such distributed generators (DGs) are interconnected to elements like energy storage units and loads together to form a micro grid. Distributed generators are the heart of micro grid applications. The distributed generators need reliable and efficient methodologies for their controlled operation. The methodologies involved in their control depend on whether DGs operated in islanding mode for feeding loads or in grid connected mode feeding active and reactive powers to the grid. The main aim of the development of such control strategies is to increase the reliability and to enhance power quality. The thesis focuses mainly on developing such methodologies that are mainly helpful for micro grid applications. Many DGs are of small capacity with low power ratings are interfaced with single phase distribution systems. For example, roof-top based PV generation systems, which are gaining prominence in distribution systems, are in general interfaced with single phase power distribution networks. The interconnection of single phase DG inverter with utility grid becomes difficult due to the inherent pulsating nature of single phase powers at double the grid frequency. In this thesis, the control strategies involve two loops in which the inner control loop is used to establish the duty ratio/modulation index for the generation of sinusoidal output current that is in phase with the grid voltage; the outer loop is used to correct the error in real and reactive powers.

 The two loop control strategies for grid interconnection is proposed in this thesis, comprises three current reference generations, namely, scalar control, modified scalar control and simplified active and reactive power control for generating the required active and reactive powers along with the separate modulation method employed, these being either asynchronous sigma delta modulation (ASDM) or model predictive control (MPC) based space vector modulation (SVM). The performance of MPC based SVM and ASDM for the control of active and reactive powers of single phase grid connected DG is verified with different current reference generation schemes. The scalar reference generation scheme results in steady state error. Though the modified scalar reference generation scheme renders zero steady state error, and it induces delay in power tracking. The MPC based SVM in combination with simplified active and reactive power control (SRPC) has the advantages of quick, accurate and stable control when compared with ASDM. Although the modified scalar reference generation scheme and SRPC have error correction mechanisms, their performance with ASDM is very poor. Therefore, the MPC based SVM with SRPC is observed to be the best combination among reference generation and modulation schemes. Though the MPC based SVM with SRPC proved to be better, there is a need of reducing the two stage to single stage as cascade loops always reduce efficiency.

 The development of single stage control strategy involves the powers to be generated as an objective function. Therefore, for the control of single phase DG to operate in grid connected mode, the powers are modelled using an MPC integrated with SVM. Further, for the operation of DG in islanding mode, the voltage is utilized as an objective function. A simple phase locked loop (PLL) free grid synchronization mechanism along with seamless transition control between grid connected mode and off-grid mode is developed. The developed MPC is integrated with SVM and examined for delivering the set-point powers in grid connection mode, supplying the local load at nominal voltage and frequency in off-grid mode and for smooth transition between these modes. The designated performance of the developed control scheme for single phase DG is confirmed through simulations, which are further validated on an experimental test bed.

 Though the achieved objectives are found to work fine for single phase designated systems, for large scale power supply single phase DGs are not suitable. Therefore, three phase systems are controlled using the objectives presented in the single phase system. However, for the large scale power generations in grid connected mode, it is observed that there is no problem in feeding power to the grid. During the islanding mode of operation in a microgrid, there may be multiple DGs. Hence, there is a need to develop a control strategy which addresses the issue of maintaining the voltage and frequency operated at nominal values while feeding the load. Also there will be rotating interface in addition to the photovoltaic operated DGs. To address these issues, a control strategy is proposed for multiple DGs coordination with a simple pulse width modulation strategy comprising of primary and secondary control. The primary control comprises modified droop control which decides the power sharing between the DGs whereas the secondary control begins restoring the voltage and frequency to nominal values if the primary control fails. The performance of the proposed control strategy is validated through simulations and hardware-in-loop (HIL) implementations using OPAL-RT.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **Sachidananda Prasad**

Title of the thesis : **Optimal Allocation of Measurement Devices for Distribution System State Estimation U Multi-Objective Evolutionary Algorithms**

Guide : **Dr. D. M. Vinod Kumar**

Degree : **Ph. D.**

Student ID No. : **714007**

**ABSTRACT**

 The power distribution networks are becoming more dynamic and complex structures than before, because of the huge integration of renewable sources, distributed energy storage, intelligent electronic devices (IED) and Smart meters (SMs). Furthermore, distribution network configuration is also changing dynamically to achieve minimum power loss and voltage deviations. Due to lack of metering infrastructure in distribution networks, real time reliable monitoring of the system becomes more challenging for power engineers. Therefore, the currently existing metering infrastructure of the distribution network needs to be modeled for reliable and secure operation of the system. Thus, the overall objective of the thesis is to design an efficient optimization model and algorithm for optimal allocation of measurement devices to improve the state estimation accuracy for real time monitoring and control of the smart distribution networks.

**The contributions of this thesis are as follows:**

1. A new multi-objective hybrid PSO-Krill Herd (KH) algorithm is proposed to optimize number and location of the measurement devices for accurate state estimation in smart distribution networks. Three objectives that need to be minimized are: (i) the total configuration cost (ii) the average relative percentage error (APE) of bus voltage magnitude and (iii) APE of bus voltage angle. As the objective functions conflict with respect to each other, a multi-objective Pareto-based non-dominated sorting hybrid PSO-KH optimization algorithm is proposed. In this approach, the random variation in loads and the metrological error of the measurement devices are also taken into account. Furthermore, the impacts of DG on state estimation performance have also been investigated.
2. A new multi-objective hybrid Estimation of distribution algorithm (EDA)-interior point method (IPM) algorithm is proposed to obtain the optimal location of measuring devices for state estimation in active distribution networks. The objective functions to be minimized are, the total network configuration cost, the average relative percentage error (APE) of bus voltage magnitude and angle estimates. As the objectives are conflicting in nature, a multi objective Pareto-based non-dominated sorting EDA has been proposed. Moreover, due to poor exploitation capability of the EDA, it is hybridized with IPM to improve its local searching ability in the search space. The hybridization of EDA and IPM brings a higher degree of balance between the exploration and exploitation capability of the algorithm during the search process. Furthermore, the loads and generators are treated as stochastic variable and the impact of different types of DGs on state estimation performance has also been investigated.
3. In distribution grids, due to the presence of different kinds of actors such as distributed generation (DG), energy storage devices systems become more complex, dynamics and uncertain in nature. Because of this changing behaviour of actors, real-time monitoring and control becomes more challenging task for the power system engineers. Thus, PMUs are of great interest because they provide synchronized measurements of voltage and current. The application of PMU for state estimation in transmission system has been widely used to improve the performance of the state estimator. Therefore it would be more advantageous to use PMU in DSSE. Therefore, in this thesis, a novel multi-objective optimization problem is proposed to find trade-offs in deployment of phrasor measurement units (PMUs) and intelligent electronic devices (IEDs) for state estimation in active distribution networks. A new hybrid estimation of distribution algorithm (EDA) has been used to find the optimal number and location of measurement devices such as PMUs and IEDs for accurate state estimation. The objective functions to be minimized in this optimization problem are the total cost of PMUs and IEDs, as well as RMS value of state estimation error. Since, the objectives are conflicting in nature, a multi-objective Pareto-based non-dominated sorting EDA algorithm is proposed. Moreover, to improve the local searching capability of the traditional EDA algorithm, the Interior point method (IPM) is hybridized with EDA to get near global optimal solution. Furthermore, the random variation in loads and generators is also considered to check the reliability of the proposed meter placement technique.
4. The robustness of the proposed multi-objective optimization model in presence of wind generators is also carried out in this thesis. All the DGs are considered as wind generators and the output of each DG is modeled using Weibull distribution function. Furthermore, tradeoffs in deployment of phasor measurement units (PMUs) and intelligent electronic devices (IEDs) for state estimation in active distribution networks is obtained. The objective functions considered to be minimized are the total cost of PMUs and IEDs as well as the RMS value of state estimation error. To get best optimal solution, multi-objective hybrid PSO-Krill Herd algorithm has been used. Moreover, the random variation in loads and generators is also considered to check the reliability of the proposed meter placement technique

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **SURESH LAKHIMSETTY**

Title of the thesis : **IMPROVISED SPACE-VECTOR PULSE WIDTH MODULATION SCHEMES FOR FOUR LEVEL OPEN-END WINDING INDUCTION MOTOR DRIVES**

Ph. D Guide : **Dr. V. T. SOMASEKHAR**

Degree : **Ph. D.**

Student ID No. : **715015**

**ABSTRACT**

 In this thesis, the Open-End Winding Induction Motor (OEWIM) drive is considered for achieving the multilevel operation. The OEWIM drive is realized by removing the star or delta connections of the stator winding of an induction motor and feeding it with two two-level Voltage Source Inverters (VSIs) from either side. In the present thesis, the VSIs are operated with two different DC input voltages, which are in the ratio of 2:1, to achieve four-levels across each motor phase winding. Thus, this drive configuration is named as the four-level Open-End Winding Induction Motor Drive.

 The four-level OEWIM drive circuit configuration mainly suffers from two problems. They are: (i) the lower dc-link voltage capacitor is overcharged by its counter-part, i.e. the higher dc-link voltage capacitor (ii) the presence of zero-sequence current (ZSC) in the motor phase windings. However, the ZSC can be avoided by denying a path for the circulation of zero-sequence current by using isolated dc-power supplies.

 This thesis investigates about the applicability of various Space-Vector Pulse Width Modulation (SVPWM) schemes for two circuit topologies of the four-level OEWIM drive (of which, one circuit is a slightly improvised version of an existing topology). The proposed SVPWM techniques avoid the overcharging of the lower-voltage dc-link capacitor and improve the drive performance. A closed-loop control strategy, based on Model Predictive Control (MPC), is also proposed to improve the performance of the OEWIM drive.

 To improve the performance of the four-level OEWIM drive, four variants of Discontinuous-Decoupled SVPWM (DDSVPWM) techniques are proposed. It is known that, the Discontinuous-SVPWM techniques reduce the switching power loss in inverters. However, lack of structural symmetry of the power circuit renders it unwieldy to devise these SVPWM schemes. Chapter-2 explores the applicability of the Discontinuous-Decoupled SVPWM techniques for the four-level OEWIMD, without compromising on the waveform symmetries. It is shown that the proposed SVPWM techniques, while avoiding the overcharging phenomenon of the low-voltage dc-link capacitor, also lower the dv/dt across the motor phase windings.

 Three variants of SVPWM strategies are proposed in Chapter-3 for the four-level OEWIM drive with two isolated dc-power supplies to reduce the switching power loss and to improve the drive performance. In the proposed SVPWM schemes, the inverter, which is operated with the lower dc-link voltage is clamped to the nearest sub-hexagonal centre (NSHC), while the other inverter is switched around it. The proposed SVPWM schemes, apart from avoiding the overcharging phenomenon and achieving all waveform symmetries, reduce power loss in the dual-inverter system (compared to the Discontinuous Decoupled SVPWM schemes available in chapter-2).

 A nested rectifier-inverter topology with two dc-power supplies (as against three reported in the earlier literature) is proposed in Chapter-4 to improve the reliability of the four level OEWIM drive. The unwanted phenomenon of overcharging the low-voltage capacitor is avoided with this power circuit also. To suppress the zero-sequence currents, an SVPWM scheme is proposed and is named as Nested Inverter Clamped Sample-Averaged Zero-Sequence Elimination (NICSAZE). The proposed NICSAZE-PWM scheme eliminates the zero-sequence currents in the average sense and reduces the power loss in the dual-inverter system.

 An improvised Predictive Current Control (PCC) algorithm, which belongs to the genre of MPC, is proposed to control the load currents of the four-level OEWIM drive in Chapter-5. The conventional PCC uses all of the available 37 candidate voltage vectors of the dual-inverter system to select the optimal voltage vector. In contrast, the proposed PCC (which utilises the concept of NSHC described in Chapter-3) requires the testing of only 5 candidate voltage vectors for the selection. Thus, the proposed PCC results in a considerable alleviation of the computational burden on the control platform. It is also shown that, compared to the conventional PCC, the proposed PCC technique results in the reduction of power loss incurred in the dual-inverter system for a considerable portion of the operating range of the drive.

 All the PWM schemes, circuit topologies and the closed-loop control strategies proposed in this thesis are first simulated using MATLAB/SIMULINK software and the results are then validated by implementing these schemes on a 5-HP, 400 V, 50 Hz, 1445 RPM, three phase open-end winding induction motor. The experimental work presented in this thesis is carried out using the dSPACE1104 control platform.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **N. VENKATAPHANENDRA BABU**

Title of the thesis : **OPTIMAL SELECTION AND PLACEMENT OF PHASOR MEASUREMENT UNITS AND THEIR APPLICATION FOR POWER SYSTEM PROTECTION**

Guide : **Dr. P SURESH BABU**

Degree : **Ph. D**

Student ID No. : **701407**

**ABSTRACT**

 The Wide Area Monitoring, Protection and Control (WAMPAC) of power systems are becoming essential tools for the system engineers in preventing blackouts. Whenever the power system operates in stressed mode and if suppose an event happens on a system element (particularly critical element), it may initiate cascading of events. At this condition, if the system engineers are unable to protect the rest of system and, control the abnormalities the system loses the power supply completely. This particular situation where the system loses generation-load balance is said to be Blackout condition. Interestingly, the WAMPAC schemes can enable the engineers to take remedial actions to avoid Blackouts by providing the synchronous data. This synchronized data will be provided by the device called Phasor Measurement Unit (PMU). So, the PMUs should be deployed in such a way that they could observe the system completely and economically. And, the process of installing of PMUs is subjected to different constraints.

 Initially, an Optimal PMU Placement scheme (OPP) is suggested to obtain the minimum number of PMUs for system complete observability. It considers the observability constraints under both normal and abnormal conditions. This OPP problem also considers zero-injection buses for placing PMUs. This algorithm applies a Binary Cuckoo Search (BCS) technique to solve the OPP problem. The suggested method is tested on few standard IEEE test systems and has been practiced for different State Level Regional power Grids (SLRGs) of the Indian power grid and United Indian Grid (UIG). The obtained results are also compared with the methods that have been already applied for standard IEEE test systems and SLRGs, and were proved to be the best and effective. Also, to maximize the observability redundancy, the second contribution introduces Optimal Placement of Phasor Measurement Units for maximizing the observability. It uses a performance index called System Observability Index (SOI) with the help of np which represents the number of the buses observed for more than one time. The proposed method is tested on few of the IEEE test systems and then applied to Southern Region of Indian power Grid(SRIG).

 The significant feature of Wide-Area Measurement System (WAMS) is to recover the data during communication failure. So, the third contribution presents a novel scheme of partitioning a PMU installed power network into a number of WAMS regions to make power system restoration process simpler. This algorithm also proposes the optimal placement of Phasor Data Concentrators (PDCs) in each region to archive the data received from PMUs. This partition considers the restoration constraints like transformer equivalent bus, generation-load balance and the observability of region for the partitioning of a power system. The proposed scheme is demonstrated with an IEEE-30 bus system, and then applied to IEEE-39, IEEE-118 bus systems and Indian Grid (IG-75) system.

 In practical substations, buses exist at different voltage levels. The bus which is being observed inside the substation should not translate to buses at other voltage levels becoming observed inside the same substation unless the tap ratios are known. And, all the methods developed were based on the thumb rule that the PMU installed bus could observe all the buses connected to it including itself even though the practical tap ratios are not known. So, the authors have assumed that the buses with different voltages can be decoupled. Unfortunately, it will increase both search space and bus number. From this, it is clear that the authors have only concentrated on reducing the number of PMUs rather than reducing substation number. To answer this, the fourth contribution has proposed the concept of optimal coverage of substation by assuming that one PMU could observe the whole substation provided the tap ratios are known. Thereafter, it introduces the identification of critical elements considering the Blackout concept. Finally, it proposes a new OPP problem considering the critical elements and the optimal substation coverage. The proposed method has been tested on some standard test systems and then applied to a practical Indian regional grid.

 The fifth contribution proposes improved line protection against single phase-ground fault using synchronized phasor data. This algorithm prevents the relay from mal-operation caused by high fault resistance. The fault detection action will be taken according to a particular phase difference relation between fault point voltage and set point voltage. This method is tested on a practical single machine single line system.

This research has successfully proposes an accurate and robust wide-area measurement system, and maximizes the observability. Then it suggests a restoration strategy for a PMU-installed power system with minimum restoration time. Later, it identifies an optimal PMU set that could observe the critical elements in power system to avoid power system Blackouts. Finally, it suggest a simple and accurate fault identification technique which is immune to fault resistance.

**ELECTRICAL & ELECTRONIC ENGINEERING**

Author : **VENKATARAMANA VEERAMSETTY**

Title of the thesis : **LOCATIONAL MARGINAL PRICE COMPUTATION FOR OPTIMAL OPERATION OF ACTIVE DISTRIBUTION SYSTEM USING GAME THEORY AND META HEURISTIC TECHNIQUES**

Guide : **Dr. CHINTHAM VENKAIAH**

Degree : **Ph. D.**

Student ID No. : **714120**

**ABSTRACT**

 As integration of Distributed Generation (DG) into the distribution system is increasing rapidly, Distribution Companies (DISCOs) need to control private DG owners and also operate DG units in such a way that optimal operation of Active Distribution System (ADS) has been achieved in terms of reduction of active power losses, emissions and improvement of reliability. DISCO can control private DG owners and also operate the network optimally in terms of reduction of active power losses, emissions and improvement of reliability by providing proper financial incentives to DG owners. Nodal pricing is one of the most efficient and important mechanisms for providing financial incentives. Computation of Locational Marginal Price (LMP) is the most prominent mechanism among all existing policies of nodal pricing. So DISCOs require an efficient tool/algorithmto compute LMP at DG buses for optimal operation of ADS. Algorithms needs to be designed in such a way that a private DG owner will receive financial incentives based on DG unit’s contribution on optimal operation of ADS. As active power load and market price are uncertain in nature, LMP computation tool which can handle uncertainties needs to be developed.

 In this thesis, Proportional nucleolus theory based iterativemethod has been developed to compute LMP at DG buses in ADS based on active power loss reduction. Proportional nucleolus theory is a cooperative game theory solution concept which has been used for allocation of change in active power losses among DG units. Financial incentives have been provided to DG owners from reduced active power loss cost. Loss sensitivity factors have been developed to find the share of active and reactive power generation at DG bus on change in active power losses. The proposed proportional nucleolus theory based iterative method provides LMP, Reactive Power Price (RPP), zero DISCO’s extra benefit due to active power loss reduction, and also estimates the state of the ADS in terms of DG units generation and active power losses. To study the robustness and effectiveness of the proposed algorithm, the proposed algorithm was implemented on 84 bus Taiwan Power Company (TPC) radial distribution system and Pacific Gas and Electric company (PG & E) 69 bus radial distribution system.

 The above mentioned proportional nucleolus theory based iterative method was further extended for computing LMP at DG buses in ADS based on active power loss and emission reduction. Proportional nucleolus theory has been used to allocate change in active power losses and emissions among DG units. Financial incentives have been provided to DG ownersfrom reduced active power loss cost and emission penalty. The proposed proportional nucleolus theory based iterativemethod provides LMP, RPP, zero DISCO’s extra benefit due to both active power loss and emission reduction, and it also estimates the state of ADS in terms of DG units generation and active power losses and emissions. The robustness and effectiveness of the proposed algorithm for LMP computation based on active power losses and emissions is verified by implementing it on 84 bus TPC radial distribution system and PG & E 69 bus radial distribution system.

 Further, a new Hybrid Genetic Dragonfly Algorithm (HGDA) based optimal power flow (OPF) has been developed to compute LMP at DG buses in ADS based on reliability improvement. First time hybridization has been done among genetic algorithm and dragonfly algorithm to get the solution closer to the global by extracting the advantages of both. This method has been developed by considering the islanded operation when line outage has occurred. Uniform price which is equal to market price is given to all DG units as part of distribution network which is connected to substation. Load and generation scheduling has been done using HGDA based OPF to compute LMP at DG buses in that part of the network which is disconnected from substation. Expected Energy Not Supplied (EENS) has been used as a reliability measuring index. In load scheduling, the weighted sum of EENS value of various type of customers has been considered as an objective function. On the other hand, in generation scheduling, weighted sum of various objectives like DISCO’s investment cost to purchase power from DG owners, active power losses and emissions in islanded portion of network has been considered as single objective function. The proposed method improves the reliability of active distribution network by providing proper incentives in terms of LMP to DG owners. The robustness and effectiveness of the proposed algorithm for LMP computation based on reliability improvement is verified by implementing the model on 38 bus and PG & E 69 bus radial distribution systems.

 Further, a new method has been developed to compute Probabilistic Locational Marginal Price (PLMP) at DG buses in ADS based on active power loss reduction by handling uncertainties that exist in load and market price. Proportional Nucleolus Theory (PNT) based iterative method has been used as deterministic approach for computing LMP values. 2m+1 scheme of point estimation method (2m+1:PEM) has been used as a probabilistic approach for handling the uncertainties. The proposed mechanism provides PLMP and Probabilistic Reactive Power Price (PRPP), and also estimates the state of the ADS in terms of active power losses which are less sensitive to randomness that exist in market price and load. The robustness and effectiveness of the proposed probabilistic approach for LMP computation based on active power loss reduction is verified by implementing it on 84 bus TPC distribution system and PG & E 69 bus radial distribution systems.

**ELECTRICAL & ELECTRONICS ENGINEERING (EEE)**

Author : **S. VENU**

Title of the thesis : **INVESTIGATION ON TRANSFORMERLESS MULTI-LEVEL INVERTER SCHEMES FOR PV SYSTEMS**

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Degree : **Ph. D**

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**ABSTRACT**

 The solar PV power generating systems are gaining importance and popularity nowadays because of its salient and inherit features like abundant zero cost fuel (sunlight), zero pollution, and less maintenance etc. However, these systems require higher initial investment which is basically due to the cost associated with the PV modules. Further, the low conversion efficiency of the PV cells (sunlight to electricity) also increases the initial investment cost. This also puts a constraint of high-efficiency operation for the power conditioning units used in the PV system. Therefore, the selection of PV inverter topology plays a critical role in minimizing the cost and efficiency of the overall PV system. Due to this reason, the transformerless PV inverter topologies are becoming more popular. These configurations can meet the above requirement satisfactorily both with respect to the cost and efficiency. However, the removal of the transformer eliminates the galvanic isolation between the PV source and output load (grid/stand-alone load). This increases the possibility for the flow of leakage current in the system. The flow of leakage current in the PV system degrades the characteristics or performance of the PV panels and also creates issues related to the safety of a person in contact with the panel. To prevent these safety-related issues, a German standard VDE 0126.1.1 has been imposed which restricts the magnitude of leakage current flowing in the PV system. Apart from meeting the VDE0126.1.1 standard, there is another requirement of feeding high quality of AC power into the grid. This objective can be fulfilled by incorporating the multi-level inverters (MLIs) in the PV power generating systems. However, in literature, many transformerless PV inverter topologies for the minimization of leakage current are proposed. However, most of the topologies discussed in the literature are restricted to a maximum of three levels in the inverter output voltage. Also, some of the topologies have other drawbacks like high device count, high switching and conduction losses etc. Thus, there is a requirement of an efficient and economical transformerless MLI topology in the PV system. This thesis proposes such MLI configurations and PWM scheme for the minimization of leakage current in the PV systems. The solutions are given for both single-phase and three-phase systems.

 To meet the objective of low cost and efficient operation, a new cascaded multilevel inverter (CMLI) for single-phase PV system is presented. The complete details of the operation of the proposed CMLI in symmetrical and asymmetrical modes along with its extension to the higher number of levels with simulation and experimental results are discussed in the thesis. The comparison of proposed CMLI with the other existing MLI topologies in the literature is also presented. However, the proposed CMLI using the existing PWM techniques requires additional circuitry to minimize the magnitude of leakage current flowing in the system.

 A new pulse width modulation (PWM) scheme is proposed for single-phase five-level CMLI for the minimization of leakage current without the addition of any extra circuitry elements is presented. The proposed CMLI is also integrated with the MPPT algorithm and is applied to a five-level CMLI. The proposed PWM technique minimizes leakage current of PV panel and the size of the electromagnetic interference filter required in the system without the addition of any switches. Furthermore, the analysis of the terminal voltage across the PV array and the common mode voltage of the inverter based on the switching function is presented. Also, the proposed PWM technique requires a reduced number of carrier waves compared to the conventional sinusoidal pulse width modulation technique for the given CMLI. However, using the proposed PWM technique for the single-phase five-level CMLI, the objective of high efficiency is not achieved.

 To overcome this drawback, a new efficient and reliable transformerless PV MLI configuration is proposed for the minimization of the leakage current in the single-phase systems. Apart from a reduced switch count, the proposed CMLI topology has additional features of low switching and conduction losses. The proposed topology with the given pulse width modulation PWM technique reduces the high-frequency voltage transitions in the terminal and common mode voltages. Furthermore, the extension of the proposed CMLI along with the PWM technique for higher levels in the output voltage is also presented. A comparison of the proposed CMLI with the existing PV multilevel inverter topologies is also presented.

 Apart from single-phase PV inverter topologies, a solution for the three-phase transformerless PV inverter topologies based on DC and NPC DC decoupling methodologies are also presented in the thesis. The new three-phase transformerless MLI topologies are presented for the minimization of leakage current. The leakage current in the three-phase MLI topology is minimized by reducing the transitions in the terminal voltage of the PV panel. The complete details of the proposed three-phase transformerless MLIs, analysis of the terminal voltage using switching functions, simulation and experimental were presented in the thesis.