NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

RULES AND REGULATIONS
SCHEME OF INSTRUCTION AND SYLLABI
FOR M.TECH PROGRAMS

Effective from 2016-17

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
WARANGAL

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

VISION

Towards a Global Knowledge Hub, striving continuously in pursuit of excellence in Education, Research, Entrepreneurship and Technological services to the society

MISSION

- Imparting total quality education to develop innovative, entrepreneurial and ethical future professionals fit for globally competitive environment.
- Allowing stake holders to share our reservoir of experience in education and knowledge for mutual enrichment in the field of technical education.
- Fostering product oriented research for establishing a self-sustaining and wealth creating centre to serve the societal needs.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Create an Educational environment to prepare the students to meet the challenges of modern electronics and communication Industry through state of art technical knowledge and innovative approaches.

MISSION

- To create learning, Development and testing environment to meet ever challenging needs of the Electronic Industry.
- To create entrepreneurial environment and industry interaction for mutual benefit.
- To be a global partner in training human resources in the field of chip design, instrumentation and networking.
- To associate with international reputed institution for academic excellence and collaborative research.

M.TECH ELECTRONICS AND COMMUNICATION ENGINEERING

SPECIALIZATION: VLSI System Design

SCHEME AND SYLLABI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY

WARANGAL

COURSE CURRICULUM FOR THE M.TECH PROGRAMME IN

VLSI SYSTEM DESIGN

RULES AND REGULATIONS

M.Tech Degree Programs

1. INTRODUCTION:

Provision of these regulations shall come into force with effect from the academic year 2014 - 2015 and shall be applicable to all M.Tech courses (unless otherwise stated) offered by the Institute.

1.1 M.Tech Degree Programs are offered in the following specializations by the respective departments as listed below:

Department	Program	Course / Specialization (s)
Civil Engineering	M. Tech	1. Engineering Structures 2.Geotechnical Engineering 3.Transportation Engineering 4. Water Resources Engg. 5. Remote Sensing and GIS 6. Environmental Engineering 7. Construction Technology and Management
Electrical Engineering	M. Tech	1. Power Systems Engineering 2. Power Electronics and Drives
Mechanical Engineering	M. Tech	1. Thermal Engineering 2. Manufacturing Engineering 3. Computer Integrated Manufacturing 4. Machine Design 5. Automobile Engineering 6. Materials and Systems Engineering Design 7. Additive Manufacturing
Electronics and Communication Engineering	M. Tech	1. Electronic Instrumentation 2. VLSI System Design 3. Advanced Communication Systems
Metallurgical and Materials Engg.	M. Tech	1. Industrial Metallurgy 2. Materials Technology
Chemical Engineering	M. Tech	1. Computer Aided Process and Equipment Design 2. Process Control
Computer Science and Engineering	M. Tech	1. Computer Science and Engineering 2. Computer Science and Information Security

1.2 The provisions of these regulations shall be applicable to any new discipline that may be introduced from time to time.

1.3The sanction of stipend will be as per the guidelines prescribed AICTE/MHRD from time to time.

2. ADMISSION:

Admissions are made on All India basis for all the programs, with reservations as per Government of India norms. The selection criterion for admission into all the M.Tech. programs is based on valid GATE score. Candidates seeking admission into M.Tech. in Engineering should have passed BE/B.Tech. or equivalent degree in the subject concerned from a recognized University/Institute with First Class not less than 60% marks or equivalent CGPA of 6.5/10. In case of SC/ST candidates 55% marks or equivalent CGPA of 6.0/10 is the eligibility requirement. Eligibility and other criteria for admissions to M. Tech. courses of the Institute will be reviewed and decided by the Senate from time to time.

3. COURSE STRUCTURE:

An M. Tech. program is of 4-semester duration, out of which 2 semester course work followed by two semester dissertation work.
The total course package for an M. Tech. Degree program will typically consist of the following components.

a) Core Courses = 32 Credits
b) Elective Courses = 18 Credits
c) Seminar and Comprehensive Viva Voce = 04 Credits
d) Dissertation = 18 Credits

a) The Departmental Board of Studies will discuss and finalize the exact credits offered for the program for the above components ‘a’ to 'd’, the semester-wise distribution of the courses and credits, as well as the syllabii of all M. Tech. Programs offered by the department from time to time and recommend the same to the Senate for consideration and approval.

b) In order to qualify for a post graduate degree of the Institute, a student is required to complete all the credits specified in the scheme of instruction for that program as approved by the Senate from time to time.

4. ACADEMIC CALENDAR:

a) The academic year is divided into two semesters.
b) The senate shall approve the schedule of academic activities for an academic year including the dates of registration, Mid semester and End semester examinations, which shall be referred to as academic calendar of the year. Each semester will normally be of 19 weeks, which includes End semester examinations. It may be ensured that the minimum number of effective teaching weeks in a semester is 16.
c) Academic calendar declared by the Senate in the beginning of a semester shall also fix fest dates during which all the co-curricular and extra-curricular programs like Technical seminars / Spring Spree/Institute day/etc. must be organized.

5. RESIDENTIAL REQUIREMENT:

The Institute is essentially residential and unless otherwise exempted/permitted, every student shall be required to reside in and be a boarder of one of the halls of residence and mess to which he/she is assigned.

6. ATTENDANCE:

Attendance in all classes (lectures/tutorials, laboratories etc.) is compulsory. A student will not be permitted to appear in the end semester examination on grounds of unsatisfactory

attendance. Minimum required attendance in each theory /laboratory course is 80% for appearing in the End Semester examination. There will not be any possibility of condoning the shortage for whatever reasons beyond this.

Attendance for both theory and laboratory courses shall be entered before the end of each working week by the concerned teacher through faculty portal of the Institute website. Students are advised to monitor the status of their attendance through student portal of the Institute website.

Absence without obtaining sanction of leave will be considered as an act of indiscipline and shall entail deduction from scholarship on pro rata basis.
No student can receive scholarship/fellowship from more than one source, either Government or Private.

7. LEAVES:

a) A post graduate student shall be entitled to the following kinds of leave during every academic year, counted from the date of commencement of the session concerned as prescribed in the academic calendar of the institute.
b) Any absence over and above the prescribed type of admissible leave shall entail deduction from the scholarship, beside other action as may be decided by the Institute.

Sl.No.	Leave	Maximum Number of days	Sanctioning authority
1.	Casual Leave	8 days per semester subjected to the condition that such leave will not be allowed for more than 6 days at a time. Casual leave cannot be combined with medical leave.	Head of the Department (HOD)
2.	Medical Leave	8 days per semester	HOD with Medical Certificate from the Institute Medical Officer.

8. REGISTRATION:

a) Every Student of the M.Tech. courses is required to be present and register at the commencement of each semester on the day fixed for and notified in the Academic calendar.
b) The registration will be organized departmentally under the supervision of the Head of the Department/ Coordinator of a respective specialization / program.
c) A student who does not register on the day announced for the purpose may be permitted, in consideration of any compelling reason, late registration within the first week on payment of additional late fee as prescribed by the Institute from time to time. Normally no late registration shall be permitted after the first week from the scheduled date.
d) Only those students will be permitted to register who have: (a) cleared all Institute and Hostel dues of the previous semesters (b) paid all required fees for the current semester, and (c) not been debarred from registering for a specified period on disciplinary action or any other ground.

e) The students will choose the subjects for registration in consultation with the Faculty Advisor. The students may also consult the Head of the Department/Division /Centre/Section/ any other teacher.

f) A student who has already registered may

(a) register for a new course in addition to the courses he/she has already registered for

(OR)

(b) opt for a new course in place of the one already registered for with the concurrence of the faculty advisor.

Any change of the course as permissible by sub-paras (a) and (b), above must however, be done within two weeks after registration.

g) A Student can register for a backlog subject either for (i) Study or for (ii) Examination. In case of Study, his / her previous marks are cancelled and will have to attend all classes and examinations along with next batch of students. Major changes in the time table shall not be entertained to accommodate backlog students. In case of registration for examination, he/she will not attend the classes, but will appear only for the end-semester examinations or make-up examinations as and when they are conducted. In such a case, the student shall be awarded only P grade, if he/she gets 40% or more marks in the end semester/makeup examination. Backlog students registering for study or examinations have to submit an undertaking that they will not change the status of their registration in the subject during the semester.

9. ASSESSMENT OF ACADEMIC PERFORMANCE:

a) There will be continuous assessment of the performance of students throughout the semester and grades will be awarded by the subject teacher.

b) Each theory subject in a semester is evaluated for 100 marks, with the following weightages.

Sub-component	**Weightage**
Continuous Evaluation	20 marks
Mid-semester Examination	30 marks
End-semester Examination	50 marks

c) The mid-semester examination will be conducted after 7 or 8 weeks of instruction. The Mid semester and End semester examinations will be conducted centrally by the examination section.

d) For assigning marks in continuous evaluation, minor(s)/surprise test/ assignment / quiz etc. may be conducted.

e) The mode and nature of the evaluation and the corresponding weightages may be intimated to the students at the beginning of the semester along with the lecture schedule.

f) Each laboratory course in a semester is evaluated for 100 marks, with the following weightages:

Sub-component	**Weightage**
Continuous evaluation (Lab report, Viva, Quiz etc.)	25 marks
Skill test	25 marks
End Semester examination	50 marks

g) COMPREHENSIVE VIVA-VOCE: The oral examination carrying 2 credits will cover the entire course of study up to I year II semester. The viva voce shall be conducted by an external examiner.

h) A Seminar Assessment Committee will be formed by the Head of the Department/Centre for the evaluation of performance at Seminars. Every student is expected to attend all the seminars of all the students of the batch held in the Department/Centre during the semester. Due weightage shall be given to a student's attendance in the overall evaluation of this requirement.

10. DISSERTATION EVALUATION:

a) 26 credits are assigned to the dissertation carried out by a student. The dissertation shall be submitted preferably by 15th June (but not earlier than 15th May). The method of evaluation is as per the guidelines given in Appendix-I.
b) The dissertation supervisor will periodically review the progress of the student and finally give his/her assessment of the work done by the student.
c) Dissertation and Viva-Voce: A student shall be required to submit a dissertation on the project work carried out by him/her. The guidelines for preparation of Dissertation shall be followed by every student as per guidelines given Appendix III. Three/four bound copies along with a soft copy of the dissertation shall be submitted to the Head of the Department/Centre within the last date prescribed in the Academic Calendar for the purpose.
d) Dissertation viva - voce will be held within the date fixed in the academic calendar and the grades will be finalized. External examiner for the evaluation of the dissertation at the end of fourth semester shall be from outside the Institution. The dissertation assessment committee constituted by the Head of the Department, along with the dissertation supervisor, shall be associated with the evaluation. The external expert who examines the Dissertation will conduct the viva voce.
e) Extension of dissertation work beyond the deadline of submission in very special case may be granted by the Dean - Academic on recommendation of the department/centre for a maximum period of 3 months. The viva-voce has to be completed within the extension period. The student shall not be eligible either for award of scholarship during the extension period or any medal/prize. However, if the student had been absent on medical grounds and his/her project had been extended, he/she may be eligible for award of medal or prize, if any. If the above mentioned extension period encroaches into the next semester, the student will have to pay the tuition fee on par with full time student.

11. DISSERTATION WORK IN COLLABORATION WITH INDUSTRY:

a) A student may, with the approval of the Head of the Department/Centre, visit an industry or a Research Laboratory for data collection, discussion of the dissertation, experimental work, survey, field studies, etc. during the project period. Projects sponsored by the industry or Research Laboratories will be encouraged and a close liaison with such organizations will be maintained.
b) A student may, with the approval of Head of the Department/Centre, do the dissertation work in collaboration with an industry, a Research and Development Organization. The student shall acknowledge the involvement and / or contribution of an industry, R&D organization in completing the project in his/her dissertation and a certificate to this effect, issued by the supervisor from the industrial organization, will be included in the dissertation.
c) It is mandatory for all students (especially those who do their project in an Industry, R&D organization in India or abroad) to make full disclosure of all data on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. Any tangible intellectual property other than copyright of dissertation may have to be assigned to the Institute. The copyright of the dissertation itself would however lie with the student as per the IPR policy in force.
d) In addition to the Supervisor from the department/centre guiding the project work, a Joint Supervisor may be appointed from the Industry and Research Laboratory with the approval of the DAC - PG &R. A certificate from the joint supervisor will be included in the dissertation. A member of faculty of the Institute, who is the internal supervisor, may, if felt necessary, visit the industry or the Research Laboratory in connection with the dissertation work of his/her student.

12. INDUSTRIAL TRAINING:

A student may undergo Industrial training for a period of eight weeks, if he/she wishes, immediately after the completion of I Year II semester.

13. EVALUATION – GRADING SYSTEM:

- As a measure of student's performance a 7-scale grading system using the following letter grades and corresponding grade points per credit shall be followed. Grading will be done based on the absolute marks obtained.

Letter Grade	**Ex**	**A**	**B**	**C**	**D**	**P**	**F**
Grade Point	**10**	**9**	**8**	**7**	**6**	**5**	**0**

No student can pass without securing at least 40% marks.
Relative grading scheme shall be followed for all the PG Programs.
The cut-off (lower limit) for EX grade should not be less than 85%.
The cut-offs for other grades between P and EX are to be fixed carefully.

- In case of bunching, the DAC-PG&R may review the reasons for bunching and modify the ranges, marginally. In all such cases, the modified ranges and the reasons should be presented to the Senate for its approval.
- In addition, there shall be four transitional grading symbols, which can be used by the examiners to indicate the special position of a student in a subject.
  - I for "Incomplete assessment", when the student misses the End- semester examination on Medical grounds (see rule 15.1).
  - R - for 'Insufficient attendance in the course (see rule 15.4).
  - W - for "Temporary withdrawal' from the Institute (see rule 19)
  - X - for "Debarred" on grounds of indiscipline /malpractices in examinations (see rule 20).

a) A semester Grade Point Average (SGPA) will be computed for each semester. The

$$SGPA = \frac{\sum_1^n C_i GP_i}{\sum_1^n C_i}$$

SGPA will be calculated as follows:
Where C_i = Credit for the course
GP_i= the grade point obtained for the course
n = Number of subjects registered for the semester.

b) Starting from I Year II Semester a Cumulative Grade Point Average (CGPA) will be computed for every student at the end of every semester.

c) The CGPA would give the Cumulative performance of the student from the I Year I semester upto the end of the semester to which it refers and calculated as follows.

$$CGPA = \frac{\sum_1^m S_i C_i}{\sum_1^m C_i}$$

Where m= total number of semesters under consideration
C_i= total number of credits registered for during a particular semester.
S_i= SGPA of the semester.

d) The CGPA, SGPA and the grades obtained in all the subjects in a semester will be communicated to every student at the end of every semester.

e) Both SGPA and CGPA will be rounded off to the second place of decimal and recorded as such. Whenever these grade point averages are to be used for the purpose of

determining the inter se merit ranking of a group of students, only the rounded off values will be used.

f) Transition Grades

(a) Grade I: When a student gets I Grade for any subject(s) during a semester, the SGPA of that semester and the CGPA at the end of that semester will be tentatively calculated ignoring this (these) subjects. After these transitional grades have been converted to appropriate grades, the SGPA for the semester and CGPA at the end of the semester will be recalculated after taking into account the new grades.

(b) About Grade F: When a student gets the 'F' grade in any subject during a semester, the SGPA and the CGPA from that semester onwards will be tentatively calculated, taking only 'zero point' for each such 'F' grade. After the 'F' grade has been substituted by better grades during a subsequent semester, the SGPA and CGPA of all the semesters starting from the earliest semester in which the 'F' grade has been updated, will be recomputed and recorded to take this change of grade into account.

(c) About grades R, W and X:When a student gets any of these transitional grades in any subject(s) during a semester, the SGPA of that semester and the CGPA at the end of that semester will be tentatively calculated by taking 'zero point' for these subject(s). After these transitional grades have been converted to appropriate grades, the SGPA for the semester and CGPA at the end of the semester will be recalculated after taking into account the new grades.

14. EXAMINATIONS:

14.1 The Institute Scholarship of a student will be withheld in case his/her CGPA at the end of any semester falls below 6.5. However, in the case of students belonging in to SC/ST it is 6.0. However, the scholarship will be restored with retrospective effect, based on recommendation of Head of the Department, the moment the CGPA crosses at least 6.5 (for SC/ST 6.0).

14.2 A student will be permitted to submit the dissertation only if he/she completes all the courses as required in the program.

14.3 Student with "F" grade is eligible to appear for makeup examination(s) as and when they are conducted by the Institute.

14.4 A student whose performance in the project work has been unsatisfactory may be assigned additional work on the same problem or assigned a new problem. If the student is assigned additional work the student will have to complete the work and appear at the viva-voce as per the academic calendar fixed by the Senate. If the student is assigned a new problem on account of any reason, the student will have to submit the dissertation and complete the viva-voce by December 31 of that calendar year. The student will not be eligible for scholarship during the extended period of his/her stay but will have to pay semester fees during the extended period of stay.

14.5 A student who has failed in the comprehensive viva-voce shall be required to present himself/herself again within a period of two months for the viva-voce on a date to be fixed by the concerned Head of the Department /Centre.

15. THE GRADES 'I' AND 'R'

a) The grade "I" may be temporarily given to a student who is unable to appear in the end semester examination because of:

(a) Illness or accident, which disables the student from appearing in the examination. This must be duly certified by the Institute Medical Officer.

(b) A calamity in the family at the time of the examination which in the opinion of the Head of the Department/Centre and Dean-Student Affairs required the student to be away from the campus.

b) If a student is unable to appear in a mid-semester examination for any of the compelling reasons mentioned above, the teacher(s) concerned may use discretion, and take a test with the same weightage.

15.3 A student who has been awarded grade 'I' in a subject in the end-semester examination shall have to appear the makeup examination as and when conducted.

15.4 A Student who has insufficient attendance in a particular subject shall be awarded grade 'R'. He/she has to re-register for that course in the subsequent semester in which it is offered.

16. MAKEUP EXAMINATION:

a) Students appearing in Makeup examination shall be governed by the following rules:
Students with "F" or "I" Grade only are eligible to write makeup examination.
Students with "R" Grade are not eligible for writing the makeup examination.
A student, who has obtained 'F' grade in makeup examination, may register for the course either for "Study" or for "Examination". (See rule 8.7).

16.2 The schedule for makeup examination is given in the Academic calendar.

16.3 A student can register for makeup examinations in any number of courses.

16.4 Students registering for examination shall be awarded only P grade, if they get 40% or more marks in the end semester/makeup examination.

16.5 Students who have registered under study mode during an academic year and have appeared for makeup examination, will be graded according to the study mode grading applicable to the regular batch of students. In case, they get an 'F' grade as per the above criteria, the students who get 40% or more marks in the make-up examination shall be awarded 'P' grade by treating them as registered under 'Examination' Mode.

17. GRADUATION REQUIREMENTS:

a) In order to qualify for a PG degree of the institute, a student:
   i) Must have completed all the credit requirements for the degree, as prescribed by the senate with grade "P" or a higher grade in each of the subjects for which the student registered in all the semesters.
   ii) Must have obtained a CGPA of at least 5.0 at the end of the semester in which the student completes all the requirements (including the dissertation) for the degree.

b) The degree will be awarded to a qualified student only after
(a) The student has cleared all Institute and Hall/Hostel dues, if any, outstanding against the student and
(b) The student has returned all library books borrowed by him/her and also returned instruments, apparatus issued to him/her in good condition.

c) A student with a CGPA of 8.0 and above, passing all subjects in the first attempt, is considered eligible for the award of First Division with Distinction.

17.4 A student with a CGPA of 6.5 and above but less than 8.0 is considered eligible for the award of First Division.

17.5 A student with a CGPA of 5.0 and above but less than 6.5 is considered eligible for the award of Second Division.

18. CONDUCT AND DISCIPLINE:

Students shall conduct themselves within and outside the precincts of the institute in a manner befitting the students of an Institute of National importance. Detailed rules regarding conduct and discipline are given in Appendix-III.

19. TEMPORARY WITHDRAWAL:

a) A student who has been admitted to M.Tech. program may be permitted to withdraw temporarily for a period of one semester or more from the Institute on account of prolonged illness/acute problem in the family provided that:

b) The student applies to the Institute within 15 days of commencement of the semester or from the last date of attending the classes, stating fully the reasons for such withdrawal together with supporting documents and endorsement of the parent/guardian.

c) The institute is satisfied that, inclusive of the period of withdrawal, the student is likely to complete all the requirements for the degree within 5 years of admission to the Program.
d) There are no outstanding dues or demand from the Institute/Department/Centre/Hall of Residence / Library.
e) A student who has been granted temporary withdrawal will be required to pay tuition fee and other fees for the current semester when the student rejoins the program.
f) A student shall be granted only one such temporary withdrawal during the program.
g) A student, who wishes to join the job, after completion of the entire course work, may be permitted to pursue his dissertation on part-time basis provided:
   i. sufficient facilities are available in the organization where he/she is working
   ii. there is a competent supervisor in the organization
   iii. the minimum period for submission of dissertation work shall be double the amount of the balance period.
   iv. the dissertation of such a part time student shall be under the guidance of two supervisors, one from the organization and the other from the Institute.

20. MALPRACTICES:

Students are not allowed to leave the Examination Hall without submitting the answer script. They will not be permitted to enter the exam hall after 30 minutes of commencement of the exam and to leave the exam hall before 30 minutes of the closure of examination.

The nature of malpractice and the minimum punishment are indicated in the following table:

Sl. No	Nature of the Malpractice	Punishment
1	Taking answer booklets out of the examination hall, used or unused.	Fine of Rs. 1000/- per paper. In case of used answer booklets. In addition to the above, the candidate shall be awarded F Grade in that subject.
2	Verbal or oral communication to neighbouring students even after warning.	Taking away the answer script and asking the student to leave the hall.
3	Possession of any incriminating material inside the examination hall (whether used or not). For example: written or printed materials, bits, writings on scale, calculator, hand kerchief, dress, part of the body and hall Ticket etc., Possession of cell phones, programmable calculator, recording apparatus or any unauthorized electronic equipment. Copying from neighbor Exchange of question papers and other materials with some answers	In case of Mid /Sessional examination, award zero marks. In case of End semester examinations, award 'F' Grade. The candidate may be allowed to write make-up examination.
4	Possession of answer book of another candidate. Giving answer book to another candidate.	The candidate shall be awarded 'F' Grade in that particular subject.
5	Misbehaviour in the examination hall (Unruly conduct, threatening the invigilator, or any other examination officials).	Cancellation of all theory examinations registered in that semester and further debarred from continuing his/her studies for one year (two subsequent

	Involved in malpractice for the second or subsequent times of serial number 2–4.	semesters). However the students are permitted to appear for makeup examinations of the previous semesters.
6	Cases of Impersonation	a)Handing over the impersonator (outsider) to the police with a complaint to take appropriate action. b)Cancelation of all examinations (all papers registered) for the bonafide student for whom the impersonation was done and further the bonafide student will be debarred from continuing his/her studies and writing all examinations for two years. c) If a student of this institute is found to impersonate a bonafide student, the impersonating student will be debarred from continuing his/her studies and writing all examinations for two years.
7	Physical assault causing injury to the invigilator or any examination officials.	Rustication from the Institute.

Any other type of malpractices reported, the enquiry committee may recommend appropriate punishment.

21. Certificate retention Fee: Students shall be charged with Certificate retention fees as per the details shown below:

All students –

- Who have passed in current and previous academic year - No charge.
- Who have passed in the last 2 to 10 academic years - Rs. 1,000
- Who have passed in the last 11 to 20 academic years - Rs. 5,000.
- Who have passed more than 20 academic years back - Rs. 10,000

22. STUDENT APPRAISAL:

It is mandatory for every student to submit the feedback on each and every course, he/she has undergone, at the end of every semester.

23. CHANGE OF REGULATIONS:

Notwithstanding all that has been stated above, the Senate, has the right to modify any of the above rules and regulations from time to time. All such modifications shall be documented and numbered sequentially and shall be made available in the Institute website for the information of the students.

ACADEMIC COMMITTEES
FUNCTIONS AND RESPONSIBILITIES

DEPARTMENTAL ACADEMIC COMMITTEE POSTGRADUATE & RESEARCH (DAC -PG&R)

Head of the Department	Chairman
All Professors of the Dept. having Ph. D.	Members
All Associate Prof. of the Dept. having Ph. D.	Members
Two Assistant prof. of the Dept. having Ph. D. (by rotation for two years)	Members

NOTE:
The Head of the department will nominate one of the members as secretary.
There shall be one DAC-PG&R for every department, which is involved in the teaching for any of the PG degree program.

FUNCTIONS:

i. To monitor the conduct of all postgraduate courses and course work of M.Tech program.
ii. To ensure academic standards and excellence of the courses offered by the department.
iii. Review and approval of the grades.
iv. To consolidate the registration of the M.Tech students and communicate to the course instructors and Dean-Academic.
v. To consider any matter related to the postgraduate program(s) of the Department and make a suitable recommendation to the Senate.
vi. To monitor the progress of research of all the candidates of the Department
vii. To forward the recommendations of the Doctoral Scrutiny Committee and the panel of External Examiners as recommended by the DSC to the Dean-Academic.
viii. To take up any responsibility or function assigned by the Senate.

DEPARTMENTAL ACADEMIC APPEALS COMMITTEE (DAAC)

Head of the Department	Chairman	
Three faculty members of the Department	Members	(1 Professor. 1 Associate Prof. and 1 Asst. Professor)
One Professor from outside the Department	Member (Nominated by Dean-Academic)	

NOTE:

- There shall be one DAAC for every department.
- The Chairman may co-opt and / or invite more members.
- If the concerned instructor is a member of DAAC then he/she shall keep himself out of the Committee during deliberations.
- The quorum for each meeting shall be a minimum of THREE (Professor from outside department is mandatory).

FUNCTIONS:

i. To receive grievance /complaints in writing from the students regarding anomaly in award of grades due to bias, victimization, erratic evaluation, etc. and redress the complaints.
ii. To interact with the concerned course instructor and the student separately before taking the decision.
iii. The decision of the DAAC will be based on simple majority

iv. The recommendations of the DAAC shall be communicated to the Dean-Academic for further appropriate action as required.

DEPARTMENTAL BOARD OF STUDIES (PG&R)

1. Head of the Department	Chairman
2. All Professors of the Department	Members
3. All Associate Professors of the Dept.	Members
4. One Professor (Allied Department)	Member
5. Two Experts	Members
(One from Industry and one from Academia)	

Note:

- All the members must possess Ph. D.
- The Chairman will nominate one of the members as secretary.
- The Chairman may co-opt and / or invite more members including external experts while framing / revising the curriculum.

FUNCTIONS:

i. To develop the curriculum for the postgraduate courses offered by the department and recommend the same to the Senate.
ii. The Board of studies is required to meet at least once in two years.

Academic Audit Committee – Department (AACD)

Director's nominee	Chairman
Head of the Department	Convener
Department nominee	Member

Functions:

- To review the internal audit reports submitted by faculty
- To recommend corrective measures, if any.
- To send a consolidated report to Academic Audit Committee – Institute

Academic Audit Committee – Institute (AACI)

Director	Chairman
Dean – Academic	Member
Two Professors nominated by Director	Members
Associate Dean – Academic Audit	Convener

Functions:

- To review the recommendations of AACD of each department
- To initiate appropriate measures (counseling/ training etc.).

APPENDIX- I
DISSERTATION EVALUATION

Dissertation Evaluation:

The evaluation of the Dissertation work carrying 26 credits, is divided into two modules:

Part-A (at the end of II Year I Semester) 8 Credits

Part-B (at the end of II Year II Semester) 18 Credits

A student has to select a topic for his/her dissertation, based on his/her interest and the available facilities at the commencement of dissertation work. The supervisor will evaluate execution of the dissertation periodically.

The dissertation report shall have to be submitted as per the approved guidelines given in Appendix-IV.

For the purpose of assessment, the performance of a student in the dissertation may be divided into the following sub components:

At the end of II Year I semester (for 8 credits)

Assessment by the supervisor	50%
Assessment by the dissertation Assessment committee of the Department	50%

At the end of IV semester (for 18 credits)

Assessment by the supervisor	50%
Assessment by the External Examiner	50%

An external examiner shall conduct the viva-voce Examination. A dissertation assessment committee constituted by the Head of the Department, along with the supervisor shall be involved in the conduct of the viva-voce examination.

APPENDIX-II

RULES RELATING TO RESIDENTIAL REQUIREMENT

1. All the students are normally expected to stay in the hostels and be a boarder of one of the messes.
2. Under special circumstances, the Director/Dean-Academic may permit a student to reside with his parent(s) within a reasonable distance from the institute. However, this permission may be withdrawn at the discretion of the Institute at any time considered appropriate without assigning any reason.
3. Married accommodation shall not be provided to any student of the undergraduate courses.
4. No student shall come into or give up the assigned accommodation in any Hall of residence without prior permission of the Chief Warden.
5. A student shall reside in a room allotted to him/her and may shift to any other only under the direction/permission of the Chief Warden.
6. Students shall be required to make their rooms available whenever required for inspection, repairs, maintenance or disinfecting and shall vacate the rooms when leaving for the vacation/ holidays.
7. Students shall be responsible for the proper care of the furniture; fan and other fittings in the rooms allotted to them and shall generally assist the Warden in ensuring proper use, care and security of those provided in the Halls for common use of all students.
8. Students will be responsible for the safe keeping of their own property. In the event of loss of any personal properly of a student due to theft, fire or any other cause the Institute shall accept no responsibility and shall not be liable for payment of any compensation.
9. Engaging personal attendants, keeping pets and use of appliances like electric heater, refrigerator, etc. by a student in Halls of Residence are prohibited.
10. All students must abide by the rules and regulations of the Halls of Residence as may be framed from time to time.
11. **It is mandatory for all ICCR students to stay in the Hostels.**

APPENDIX-III
STUDENTS' CONDUCT AND DISCIPLINARY CODE

It is the responsibility and duty of each and every student of the Institute to become acquainted with "Students Conduct and Disciplinary Code". It is presumed that every student from the date of his/her admission to the Institute has knowledge of this code. All students are required to strictly adhere to this code as a condition of their admission to the Institute and these rules would be binding on and enforceable against them or any one among them.

Section 1: Responsibilities of the Students

It shall be the responsibility of the students

a) To behave and conduct themselves in the Institute campus, hostels and premises in a dignified and courteous manner and show due respect to the authorities, employees and elders.

ii) To follow decent and formal dressing manners. Students should avoid clothing depicting illegal drugs, alcohol, prophane language, racial, sexual and vulgar captions etc.

iii) To access all educational opportunities and benefits available at the Institute and make good use of them to prosper academically and develop scientific temper.

iv) To respect the laws of the country, human rights and to conduct in a responsible and dignified manner at all times.

v) To report any violation of this Code to the functionaries under this Code.

Section 2: Behaviour of the Students

1. Groupism of any kind that would distort the harmony is not permitted.
2. Students are expected to spend their free time in the Library. They shall not loiter along the verandas or crowd in front of the offices or the campus roads. Students should refrain from sitting on places such as parapets, stairs, footpaths etc.
3. Possession or consumption of narcotic drugs and other intoxicating substances are strictly prohibited in the campus and hostels.
4. Silence shall be maintained in the premises of the Institute.
5. Students are not permitted to use mobile phones in the class room, library, computer centre, examination halls, etc.
6. **Students shall refrain from all activities considered as ragging which is a criminal offence.**
7. Students are prohibited from indulging in anti-institutional, anti-national, antisocial, communal, immoral or political expressions and activities within the campus and hostels.
8. Politically based students' and other organizations or outfits are not allowed in the campus. Students are strictly prohibited from organizing, attending or participating in any activity or agitation sponsored by politically based organizations.
9. Students shall not deface, disfigure, damage or destroy or cause any loss in any manner to all the public, private or Institute properties.
10. Without specific permission of the authorities, students shall not bring outsiders to the Institute or hostels.
11. No one shall bring, distribute or circulate unauthorized notices, pamphlets, leaflets etc within the campus or hostels. The possession, distribution or exhibition of any item by any means which is *per se* obscene is prohibited within the campus or on any property owned/ managed by the Institute.
12. No student shall collect money either by request or by coercion from others within the campus or hostels.
13. The Institute being a place of learning and an exclusive academic zone, nobody shall respond to any call for any form of strike, procession or agitation including slogan shouting, *dharna, gherao,* burning of effigy or indulge in anything which may harm the peaceful atmosphere of the Institution and shall eschew from violence in the campus and hostels and even out side.
14. Possession or usage of weapons, explosives or anything that causes injury/ damage to the life and limb or body of any human being or property is prohibited.
15. **Use of motorized vehicles within the Institute premises is strictly prohibited.**
16. Students shall only use the waste bins for dispensing waste materials within the campus including classrooms, hostels, offices, canteen and messes.
17. Any conduct which leads to lowering of the esteem of the Institute is prohibited.
18. **Any unauthorized tour/visit by individual or group of students shall be treated as a serious conduct violation and all such students will be imposed disciplinary penalties.**

Section 3: Disciplinary Sanctions

Any student exhibiting prohibited behaviour mentioned in this Code shall, depending upon the gravity of the misconduct or depending on its recurrence, be subjected to any of the following disciplinary sanctions. Any student who is persistently insubordinate, who is repeatedly or wilfully mischievous, who is guilty of fraud, in the opinion of the competent authority, is likely to have an unwholesome influence on his/ her fellow students, will be removed from the rolls.

I. Minor Sanctions

i. Warning or Reprimand: This is the least sanction envisaged in this Code. The student engaged in any prohibited behaviour will be issued a warning letter.

ii. Tendering Apology: The student engaged in any prohibited behaviour may be asked to tender an apology for his/her act and undertaking that he/she shall not indulge in such or any of the prohibited behaviour in future.

II. Major Sanctions

i. Debarring from Examinations: A student/group of students may be debarred from writing all/any/some of the examinations, which forms part of the academic program for which he/she/they has/ have joined.

ii. Suspension: A student may be suspended from the Institute for violation of any of the provisions of this Code. The period of suspension and conditions, if any, shall be clearly indicated in the communication addressed to the student. The student shall lose his/her attendance for the suspended period.

iii. Restitution: Restitution implies reimbursement in terms of money and/or services to compensate for personal injury or loss, damage/disfiguration to property of the Institute or any property kept in the premises of the Institute in any manner. The students/group of students may be asked to compensate for the loss that has been caused to any person or property of the Institute or any property kept in the premises of the Institute due to the act of vandalism perpetrated by the students. The students/group of students shall also be liable to put in their service to restore any loss or damage caused to any property and thereby bringing it to its original form if it is possible.

iv. Forfeiture: Caution deposit of any student engaged in any prohibited behaviour shall be forfeited.

v. Expulsion: This is the extreme form of disciplinary action and shall be resorted to only in cases where stringent action is warranted. Expulsion is the permanent dismissal of a student from the Institute. Such a student will not be eligible for readmission to any of the courses of this Institute.

Section 4: Functionaries under the Code

i) Heads of the Departments/ Faculty Advisors/Chief Warden/ Wardens of Hostels: As the persons in charge of the Departments/Hostels, the respective functionaries of all Teaching Departments and Hostels shall have the power and duty to take immediate action to curb any prohibitory behaviour as envisaged under this code. As these functionaries cannot single handedly manage all the issues, they can assign part of the work to the teachers and the teachers of all the departments/wardens have the responsibility to inform any incident of prohibited behaviour to the Heads of the Departments/ Chief Warden so that any serious issue can be settled before the same goes out of control. The Head of the Departments/ Chief Warden shall have the power to impose minor sanctions as envisaged under section 3(I) of this Code.

They can also recommend imposition of major sanctions as envisaged under Section 3(II) of this Code to the Director. The Head of the Departments/ Faculty Advisors/Chief Warden/ Wardens of Hostels while taking any action as envisaged in the code shall do so in an impartial manner and see to it that the sanction imposed/proposed is commensurate with the gravity of the prohibited behaviour. Any lapse on the part of a teacher/ Warden to report any instance of violence and misconduct on the part of the students shall be reported to the Director by the respective Head of the Departments/Chief Warden. The Wardens of Hostels shall be responsible for maintaining strict discipline and decorum in the hostel. He/she shall specifically see to it that the inmates of the hostel do not involve themselves in violation of any clause under Section 2 of this Code.

ii) Deans

Any authority of the Institute with delegated powers shall have the power to visit/inspect any premises, buildings or any property of the Institute when there is a genuine doubt that any act of prohibited behaviour is taking place and can take any lawful actions to curb such behaviour. The HODs/ Faculty Advisors/Chief Warden/ Wardens of Hostels shall report to the Dean (Students) any instances of prohibited behaviour, who in turn shall bring it to the notice of the Director. The Dean (Students) shall forward the

recommendations from the HODs/ Chief Warden to impose a major sanction under Section 3(II) of this Code to the Director after noting his observations. The Dean (Students) can also *suo moto* recommend action against any student/students indulging in prohibited behaviour which is brought to his/ her notice.

iii) Director

The Director shall be the ultimate authority in imposing major sanctions as envisaged under Section 3(II) against the students for acts of prohibited behaviour. The Director can also entertain any appeal from any student/students aggrieved by the action of any authority of the Institute under or subordinate to the Director and decide the case on merit.

Section 5: Right to Appeal

The student/students aggrieved by the action of any authority of the Institute under or subordinate to the Director can appeal to the Director and any student aggrieved by the action of the Director can appeal to the Senate. The decision of the Senate shall be final and binding on the students.

Section 6: Assistance from Law Enforcement Agencies

The Deans/ HoDs/ Chief Warden shall have the power and duty to call the Police immediately with the concurrence of the Director when there is a threat of Law and Order situation in the Campus and also when there is a genuine apprehension that any incident of rioting, vandalism or any other act prohibited by law is likely to take place. The Deans/ HoDs/ Chief Warden shall in such a case give a detailed report to the Director. The Director/ Deans/ HoDs/ Chief Warden can also arrange for video recording of the entire situation and take requisite actions through police and other concerned authorities.

Section 7: Grievance Redressal Committee

The Institute will also set up “Grievance Redressal Committee” where the students can air their grievances. The Committee shall consist of the Deans/ HoDs/ Chief Warden and also members of the Parent-Teacher Association. Till these committees are constituted, *ad-hoc* committees shall be formed by the Director.

Section 8: Undertaking by the Students

The students joining any academic program of the Institute will have to give an undertaking to the effect that he/she will comply with the provisions envisaged in this Code in letter and spirit and even if it is not given them as well, will be bound by the provisions of this Code.

Section 9: Opportunity for Hearing

No order other than the order suspending or warning a student shall be passed without giving an opportunity of hearing to the Student/ Students.

Section 10: Ultimate Authority

For all disciplinary matters related to students, the Director shall be the ultimate authority as provided herein.

Section 11: Amendments to the Code

The Senate of the Institute shall have the power to amend any of the provisions in this Code. The amendments shall be brought to the notice of the students and faculty of the Institute through notice put on the Institute web site, notice boards of the Institute or through emails.

APPENDIX-IV
GUIDELINES FOR PREPARATION OF DISSERTATION REPORTS

Preamble

While utmost attention must be paid to the content of the dissertation report, which is being submitted in partial fulfilment of the requirements of the M.Tech degree, it is imperative that a standard format be prescribed. The same format shall also be followed in preparation of the final soft copies to be submitted to the Library in future.

1. Organization of the Dissertation

The dissertation report shall be presented in a number of chapters, starting with Introduction and ending with Summary and Conclusions. Each of the other chapters will have a precise title reflecting the contents of the chapter. A chapter can be subdivided into sections, subsections and sub-subsection so as to present the content discretely and with due emphasis. When the work comprises two or more mutually independent investigations, the dissertation report may be divided into two or more parts, each with an appropriate title. However, the numbering of chapters will be continuous right through, for example Part 1 may comprise Chapters 2 - 5, Part 2, Chapters 6 - 9.

1.1 Introduction

The title of Chapter 1 shall be Introduction. It shall justify and highlight the problem posed, define the topic and explain the aim and scope of the work presented in the dissertation report. It may also highlight the significant contributions from the investigation.

1.2 Review of Literature

This shall normally form Chapter 2 and shall present a critical appraisal of the previous work published in the literature pertaining to the topic of the investigation. The extent and emphasis of the chapter shall depend on the nature of the investigation.

1.3 Report on the present investigation

The reporting on the investigation shall be presented in one or more chapters with appropriate chapter titles. Due importance shall be given to experimental setups, procedures adopted, techniques developed, methodologies developed and adopted. While important derivations/formulae should normally be presented in the text of these chapters, extensive and long treatments, copious details and tedious information, detailed results in tabular and graphical forms may be presented in Appendices. Representative data in table and figures may, however, be included in appropriate chapters. Figures and tables should be presented immediately following their first mention in the text. Short tables and figures (say, less than half the writing area of the page) should be presented within the text, while large table and figures may be presented on separate pages. Equations should form separate lines with appropriate paragraph separation above and below the equation line, with equation numbers flushed to the right.

1.4 Results and Discussion

This shall form the penultimate chapter of the dissertation report and shall include a thorough evaluation of the investigation carried out and bring out the contributions from the study. The discussion shall logically lead to inferences and conclusions as well as scope for possible further future work.

1.5 Summary and Conclusions

This will be the final chapter of the dissertation report. A brief report of the work carried out shall form the first part of the Chapter. Conclusions derived from the logical analysis presented in the Results and Discussions Chapter shall be presented and clearly

numerated, each point stated separately. Scope for future work should be stated lucidly in the last part of the chapter.

1.6 Appendix

Detailed information, lengthy derivations, raw experimental observations etc. are to be presented in separate appendices, which shall be numbered in Roman Capitals (e.g. “Appendix IV”). Since reference can be drawn to published/unpublished literature in the appendices these should precede the “Literature Cited” section.

1.7 Literature Cited

This should follow the Appendices, if any, otherwise the Summary and Conclusions chapter. The candidates shall follow the style of citation and style of listing in one of the standard journals in the subject area consistently throughout his/her report, for example, IEEE in the Department of Electrical Engineering, Materials Transactions in Department of Metallurgical Engineering and Materials Science. However, the names of all the authors along with their initials and the full title of the article/monogram/book etc. have to be given in addition to the journals/publishers, volume, number, pages(s) and year of publication. Citation from websites should include the names(s) of author(s) (including the initials), full title of the article, website reference and when last accessed. Reference to personal communications, similarly, shall include the author, title of the communication (if any) and date of receipt.

1.8 Publications by the candidate

Articles, technical notes etc. on the topic of the dissertation report published by the candidate may be separately listed after the literature cited. This may also be included in the contents. The candidates may also include reprints of his/her publications after the literature citation.

1.9 Acknowledgements

The acknowledgments by the candidate shall follow the citation of literature, signed by him/her, with date.

2. DISSERTATION FORMAT

2.1 Paper

2.1.1 Quality: The dissertation report shall be printed / photo copied on white bond paper, whiteness 95% or above, weight 70 gram or more per square meter.

2.1.2 Size: The size of the paper shall be standard A4; height 297 mm, width 210 mm.

2.1.3 Type Setting,Text Processing and Printing: The text shall be printed employing Laserjet or Inkjet printer, the text having been processed using a standard text processor. The standard font shall be Times New Roman of 12 pts with 1.5 line spacing.

2.1.4 Page Format: The Printed Sheets shall have the following written area and margins:

Top Margin 15 mm
Head Height 3 mm
Head Separation 12 mm
Bottom Margin 22 mm
Footer 3 mm
Foot Separation 10 mm
Text Height 245 mm
Text Width 160 mm
When header is not used the top margin shall be 30 mm.

Left and Right Margins
Single sided
Left Margin 30mm

Right Margin 20 mm

2.1.5 Pagination: Page numbering in the text of the report shall be Hindu Arabic numerals at the centre of the footer. But when the candidate opts for header style the page number shall appear at the right and left top corner for the odd and even number pages, respectively. Page number "1" for the first page of the Introduction chapter shall not appear in print, only the second page will bear the number "2". The subsequent chapters shall begin on a fresh page. When header style is chosen the first page of each chapter will not have the header and the page number shall be printed at the centre of the footer. Pagination for pages before the Introduction chapter shall be in lower case Roman numerals, e.g., "iv".

2.1.6 Header: When the header style is chosen, the header can have the Chapter number and Section number (e.g., Chapter 2, Section 3) on even numbered page headers and Chapter title or Section title on the odd numbered page header.

2.1.7 Paragraph format: Vertical space between paragraphs shall be about 2.5 line spacing. The first line of each paragraph should normally be indented by five characters or 12mm. A candidate may, however, choose not to indent if he/she has provided sufficient paragraph separation. A paragraph should normally comprise more than one line. A single line of a paragraph shall not be left at the top or bottom of a page (that is, no windows or orphans should be left). The word at the right end of the first line of a page or paragraph should, as far as possible, not be hyphenated.

2.2 Chapter and Section Format

2.2.1 Chapter: Each chapter shall begin on a fresh page with an additional top margin of about 75mm. Chapter number (in Hindu-Arabic) and title shall be printed at the centre of the line in 6mm font size (18pt) in bold face using both upper and lower case (all capitals or small capitals shall not be used). A vertical gap of about 25mm shall be left between the Chapter number and Chapter title lines and between chapter title line and the first paragraph.

2.2.2 Sections and Subsections: A chapter can be divided into Sections, Subsections and Sub-sub Sections so as to present different concepts separately. Sections and subsections can be numbered using decimal points, e.g. 2.2 for the second section in Chapter 2 and 2.3.4 for the fourth Subsection in third Section of Chapter 2. Chapters, Sections and Subsections shall be included in the contents with page numbers flushed to the right. Further subsections need not be numbered or included in the contents. The Section and Sub-Section titles along with their numbers in 5 and 4mm (16 and 14 pt) fonts, respectively, in bold face shall be flushed to the left (not centred) with 15 mm space above and below these lines. In further subdivisions character size of 3 and 3.5 with bold face, small caps, all caps and italics may be used for the titles flushed left or centred. These shall not feature in the contents.

2.2.3 Table / Figure Format: As far as possible, tables and figures should be presented in portrait style. Small size table and figures (less than half of writing area of a page) should be incorporated within the text, while larger ones may be presented on separate pages. Table and figures shall be numbered chapter wise.

For example, the fourth figure in chapter 5 will bear the number Figure 5.4 or Fig 5.4 Table number and title will be placed above the table while the figure number and caption will be located below the figure. Reference for Table and Figures reproduced from elsewhere shall be cited in the last and separate line in the table and figure caption, e.g. (after McGregor[12]).

3 Auxiliary Format

3.1 Binding: The evaluation copies of the dissertation report may be spiral bound or soft bound. The final hard bound copies to be submitted after the viva-voce examination will be accepted during the submission of dissertation report with the following colour specification:

M.Tech. Dissertation (Gray)

3.2 Front Covers: The front covers shall contain the following details:
Full title of report in 6 mm 22 point's size font properly centred and positioned at the top. Full name of the candidate in 4.5 mm 15 point's size font properly centred at the middle of the page. A 40 mm dia replica of the Institute emblem followed by the name of department, name of the Institute and the year of submission, each in a separate line and properly centred and located at the bottom of page.

3.2.1 Lettering: All lettering shall be embossed in gold.

3.2.2 Bound back: The degree, the name of the candidate and the year of submission shall also be embossed on the bound (side) in gold.

3.3 Blank Sheets: In addition to the white sheets (binding requirement) two white sheets shall be put at the beginning and the end of the report.

3.4 Title Sheet: This shall be the first printed page of the Dissertation and shall contain the submission statement: the Dissertation Report submitted in partial fulfilment of the requirements of the M.Tech Degree, the name and Roll No. of the candidate, name(s) of the Supervisor and Co-supervisor(s) (if any), Department, Institute and year of submission.
Sample copy of the 'Title Sheet' is appended (Specimen 'A').

3.5 Dedication Sheet: If the candidate so desires(s), he/she may dedicate his/her report, which statement shall follow the title page. If included, this shall form the page 1 of the auxiliary sheets but shall not have a page number.

3.6 Approval Sheet: In the absence of a dedication sheet this will form the first page and in that case shall not have a page number. Otherwise, this will bear the number two in Roman lower case “ii” at the centre of the footer. The top line shall be:

Dissertation Approval for M.Tech

A sample copy of the Approval Sheet is appended (Specimen `B')

3.7 Abstract: The 500 word abstract shall highlight the important features of the dissertation report and shall correspond to the electronic version to be submitted to the Library for inclusion in the website. The Abstract in the report, however, shall have two more parts, namely, the layout of the report giving a brief chapter wise description of the work and the key words.

3.8 Contents: The contents shall follow the Abstract and shall enlist the titles of the chapters, section and subsection using decimal notation, as in the text, with corresponding page number against them, flushed to the right.

3.8.1 List of Figures and Tables: Two separate lists of Figure captions and Table titles along with their numbers and corresponding page numbers against them shall follow the Contents.

3.9 Abbreviation Notation and Nomenclature: A complete and comprehensive list of all abbreviations, notations and nomenclature including Greek alphabets with subscripts and superscripts shall be provided after the list of tables and figures. As far as possible, generally accepted symbols and notation should be used.
Auxiliary page from dedication (if any) to abbreviations shall be numbered using Roman numerals in lower case, while the text starting from the Introduction shall be in Hindu Arabic.
The first pages in the both the cases shall not bear a page number.

3.10 A Declaration of Academic Honesty and Integrity: A declaration of Academic honesty and integrity is required to be included along with every dissertation report after the approval sheet. The format of this declaration is given in Specimen ‘C' attached.

****

Specimen 'A': Title Sheet

(Title)

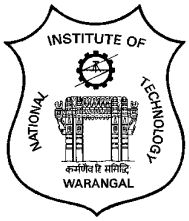
Submitted in partial fulfilment of the requirements
of the degree of
(Master of Technology)
by
(Name of the Student)
(Roll No._____)

Supervisor (s):

_____

_____

_____



(Name of the Department)
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL
(Year)

Specimen `B': Approval Sheet

This dissertation entitled (Title) by (Author Name) is approved for the degree of _____ (Degree details).

Examiners

_____

_____

_____

Supervisor (s)

_____

_____

_____

Chairman

_____

Date :_____

Place :_____

Specimen `C' – Declaration

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

_____

(Signature)

_____

(Name of the student)

_____

(Roll No.)

Date: _____

Specimen `D' – Certificate

This is to certify that the dissertation work entitled " *name of the dissertation* " is a bonafide record of work carried out by "*Mr/Ms name of the student with Roll No.*", submitted to the faculty of "*name of the department* ", in partial fulfilment of the requirements for the award of the degree of Master of Technology in "*name of the program*" at National Institute of Technology, Warangal during the academic year ----------.

Name of the HOD
Head of the Department
Department of ----------
NIT Warangal

Name of the Supervisor
Designation
Department of ------
NIT Warangal

Graduate Attributes

These Graduate Attributes are identified by National Board of Accreditation.

1. Scholarship of Knowledge: Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

2. Critical Thinking: Analyze complex engineering problems critically, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

3. Problem Solving: Think laterally and originally, conceptualize and solve engineering problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

4.Research Skill: Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

5. Usage of modern tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

6. Collaborative and Multidisciplinary work: Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

7. Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economic and financial factors.

8.Communication: Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

9. Life-long Learning: Recognize the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

10. Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

11. Independent and Reflective Learning: Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.TECH IN VLSI-SYSTEM DESIGN

Program Education Objectives

PEO 1	Design and generate GDS files for digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, algorithms and develop testing methods.
PEO 2	Model passive and active devices suiting advances in IC fabrication technology.
PEO 3	Design low power and improved performance VLSI signal processing architectures and implement them on FPGA platforms.
PEO 4	Communicate effectively and convey ideas using innovative engineering tools.
PEO 5	Perceive lifelong learning as a means of enhancing knowledge base and skills necessary to contribute to the improvement of their profession and community.

Mapping of Mission statements with program educational objectives

Mission	PEO1	PEO2	PEO3	PE04	PEO5
To create learning, development and testing environment to meet ever challenging needs of the Electronic industry.	3	3	3	2	2
To create entrepreneurial environment and industry interaction for mutual benefit.	2	2	2	3	3
To be a global partner in Training the human resource in the fields of Chip Design, Instrumentation and Networking.	2	3	2	2	3
To associate with internationally reputed Institutions for academic excellence and collaborative research.	2	2	2	2	3

Mapping of program educational objectives with graduate attributes

PEO	GA1	GA2	GA3	GA4	GA5	GA6	GA7	GA8	GA9	GA10	GA11	GA12
PEO1	3	2	-	2	-	-	1	3	-	2	-	2
PEO2	3	1	-	1	-	1	2	3	-	2	2	2
PEO3	2	1	3	3	3	2	3	3	2	2	3	2
PEO4	3	3	2	-	3	2	3	3	3	3	3	3
PEO5	2	2	3	3	3	-	-	3	-	2	-	2

Program Outcomes

PO1	Identify, characterize, model and offer solutions to issues related to IC design
PO2	Understand the advances in the VLSI technologies
PO3	Identify design requirements of analog and mixed signal circuits
PO4	Design low power digital integrated circuits
PO5	Develop efficient architectures for improving system performance in terms of speed, power consumption, and accuracy.
PO6	Perform all design functions using EDA tools.
PO7	Specify appropriate physical design automation algorithm meeting system requirements.
PO8	Develop test strategies suitable for the integrated circuits in analog and mixed signal domain.
PO9	Communicate technical material through formal written reports satisfying accepted standards of writing style while adopting professional ethics
PO10	Work in a team effectively with improved communication skills.
PO11	Understand how organizations work, generate wealth, manage finances and effectively utilize human resources.
PO12	Develop lifelong learning methods.

Mapping of POs and PEOs

	PEO1	**PEO2**	**PEO3**	**PEO4**	**PEO5**
PO1	3	3	2	1	2
PO2	2	3	2	1	2
PO3	3	2	2	1	2
PO4	2	2	3	1	2
PO5	2	2	3	1	2
PO6	3	1	1	1	2
PO7	3	1	2	1	2
PO8	3	3	1	1	2
PO9	1	1	1	3	2
PO10				3	2
PO11				3	
PO12	1	1	1	2	3

Detailed Course Structure

I Year-I Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	MA5017	Computational Techniques in Microelectronics	3	0	0	3
2	EC5201	Device Modelling	3	0	0	3
3	EC5202	Digital IC Design	4	0	0	4
4	EC5203	Analog IC Design	4	0	0	4
5		Elective - I	3	0	0	3
6		Elective - II	3	0	0	3
7	EC5204	Analog IC Design Laboratory	0	0	6	4
8	EC5205	Digital IC Design Laboratory	0	0	3	2
Total			**20**	**0**	**9**	**26**
I Year-II Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	EC5251	Testing and Testability	3	0	0	3
2	EC5252	Mixed Signal Design	4	0	0	4
3	EC5253	RF IC Design	3	0	0	3
4		Elective - III	3	0	0	3
5		Elective - IV	3	0	0	3
6		Elective - V	3	0	0	3
7	EC5254	Mixed Signal Design Laboratory	0	0	6	4
8	EC5255	Physical Design Automation Laboratory	0	0	3	2
9	EC5291	Seminar	0	0	3	2
Total			**19**	**0**	**12**	**27**
II Year-I Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	EC6241	Comprehensive Viva-voce	0	0	0	4
2	EC6249	Dissertation Part-A	0	0	0	8
Total			**0**	**0**	**0**	**12**
II Year-II Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	EC6299	Dissertation Part-B	0	0	0	18
Total			**0**	**0**	**0**	**18**

List of Electives						
S.No	**Cour No**	**Course Name**	**L**	**T**	**P**	**C**
Elective - I	EC5211	Microchip Fabrication Techniques	3	0	0	3
	EC5212	Clean room Technology and Maintenance	3	0	0	3
	EC5213	ULSI Technology	3	0	0	3
Elective - II	EC5214	VLSI DSP Architectures	3	0	0	3
	EC5215	Hardware/Software Co-design	3	0	0	3
	EC5216	Hardware Description Languages	3	0	0	3
Elective - III	EC5261	FPGA Design	3	0	0	3
	EC5262	Full Custom Design	3	0	0	3
	EC5263	ASIC System Design	3	0	0	3
Elective - IV	EC5264	Low Power VLSI Design	3	0	0	3
	EC5265	Ga As Technology	3	0	0	3
	EC5266	Formal Verification	3	0	0	3
Elective - V	EC5267	CAD for VLSI	3	0	0	3
	EC5268	MEMS & Microsystems	3	0	0	3
	EC5269	Physical Design Automation	3	0	0	3

Credit Structure					
Category	**I SEM**	**II SEM**	**III SEM**	**IV SEM**	**Total**
Core courses	14	10	0	0	24
Electives	6	9	0	0	15
Lab Courses	6	6	0	0	12
Comprehensive Viva-Voce	0	0	4	0	4
Seminar	0	2	0	0	2
Project	0	0	8	18	26
Total	**26**	**27**	**12**	**18**	**83**

MA5017	Computational Techniques in Microelectronics	PCC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Formulate problem in terms of finite elements
CO2	Estimate the errors in the proposed solutions
CO3	Generate the grid required for the problem
CO4	Apply FEM, FVM methods to analyse ICs.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	1	2	1						1
CO2		1	2	1		2	2					1
CO3		3	1	1	1	1						2
CO4				1			1					1

Detailed syllabus

Numerical solution of differential equations: FEM, FVM, FDM. Linear circuit simulation techniques: Forward Euler Approximation, Backward Euler Approximation, Trapezoidal Approximation, One Step Integration Approximation

Non-linear circuit simulation techniques: Non Linear DC analysis, Newton RaphsonIteration, Multi-Dimensional Newton RaphsonIteration. Error estimates, Transient and small signal solutions, Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

Introduction to physical design : VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles.

Reading:

1. L.O.Chua and P.M.Lin, Computer Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques, Prentice Hall, 1975.
2. Pallage, R.Rohrer and C.Visweswaraiah, Electronic Circuit and System Simulation Methods, McGrawHill, 1995.
3. NaveedShewani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.

EC5201	Device Modeling	PCC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Formulate MOSFET models for long channel devices
CO2	Update the models to overcome short channel issues
CO3	Evaluation of performance metrics for active devices
CO4	Establish current voltage distribution in active devices

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	1	1	3						3
CO2	2	3	1	1	1	2						2
CO3	2	3	2	2	1	1						3
CO4	1	2	1	1	1	1						3

Detailed syllabus
Basic Device Physics: Energy bands in solids, p-n Junctions, MOS Capacitors, Metal-Silicon Effects, MOSFET Devices Design: Long Channel MOSFET, Short-Channel MOSFETS, MOSFET Scaling, Threshold Voltage. MOSFET DC Model: Drain Current Calculations, Pao-Sah Model, Charge Sheet Model, Piece-Wise Drain Current Model for Enhancement Devices

CMOS Performance Factors: Basic CMOS Circuit Elements, Parasitic Elements, Sensitivity of CMOS delay to device parameters, Performance Factors of Advanced CMOS Devices.

Bipolar Devices Design: npn&pnp Transistors, Ideal Current-Voltage Characteristics, Bipolar Device Models for Circuit and Time-Dependent Analyses, Modern Bipolar Transistor Structures, Figures of Merit of a Bipolar Transistors, Digital Bipolar Circuits

MOSFET DC Model: Drain Current Calculations, Pao-Sah Model, Charge Sheet Model, Piece-Wise Drain Current Model for Enhancement Devices.

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Reading:
1. M.S. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley, 2008.
2. Ben G Streetman, Solid State Electronic Devices, 6th Edition, Pearson Prentice-Hall, 2009.
3. Yuan Taur and T H Ning, Fundamentals of Modern VLSI Devices, 2nd Edition, Cambridge

EC5202	Digital IC Design	PCC	4 – 0 – 0	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Design CMOS inverters with specified noise margin and propagation delay.
CO2	Synthesize digital circuit using HDLs.
CO3	Implement efficient techniques at circuit level for improving power and speed of digital circuits
CO4	Design a processor meeting timing constraints.
CO5	Design semiconductor memories to improve access times and power consumption.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	2	3	2							1
CO2	2	1	1	1	2	2	1					
CO3	2	1	1	2	3	1		1				1
CO4	1	1	2	2	2	1	2	1				
CO5	1	1	1	2	3			1				

Detailed syllabus

MOS INVERTERS: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations

DESIGNING COMBINATIONAL LOGIC GATES in CMOS: Introduction, Static CMOS Design, Dynamic CMOS Design, Power Consumption in CMOS Gates.

DESIGNING SEQUENTIAL LOGIC GATES in CMOS: Introduction, Static Sequential Circuits Dynamic Sequential Circuits, Non-Bistable Sequential Circuits, Logic Style for Pipelined Structures. Timing Issues in Digital Circuits**:** Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization.

DESIGNING ARITHMETIC BUILDING BLOCKS: Introduction**,** The Adder: Definition, Circuit and Logic Design, The Multiplier: Definition**,** The Shifter: Definition**,** Power Considerations in Data path Structures.Designing Memory**:** Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM**,**Memory Peripheral Circuitry

Reading:
1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.
2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

EC5203	ANALOG IC DESIGN	PCC	4 – 0 – 0	4 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the significance of different biasing styles and apply them for different circuits.
CO2	Design basic building blocks of analog ICs up to layout level.
CO3	Develop a procedure for optimal compensation of op-amp against process, supply and temperature variations
CO4	Identify suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system
CO5	Design an optimally compensated Op-amp including parasitic effects upto tape-out

Mapping of course outcomes with program outcomes:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3		2	1		1				3
CO2	2	1	3		2	2		1				2
CO3	2	1	3		2	1						
CO4	1	1	3		3	2						
CO5	1	1	3		2	1						2

Detailed syllabus

MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices.

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references.

Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, Cascode, folded cascode, choice of device models.

Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, replication principle, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion. Operational amplifier-characterization, Two-stage OP amp, process and temperature independent compensation, output stage.

Reading:

1. P R Gray and R G Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

EC5211	MICROCHIP FABRICATION TECHNIQUES	DEC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Comprehend impact of semiconductor industry on the design of development of integrated circuits.
CO2	Acquaint with clean room technology
CO3	Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
CO4	Specify NMOS and CMOS design rules corresponding to 180nm, 90nm, 45 nm technologies
CO5	Understand packaging principles

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2		1			1					1
CO2	1	1										1
CO3	1	1		1		1	1					
CO4	2	2	1	1								1
CO5	1	1										

Detailed syllabus

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.

Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping, Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

Reading:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

EC5212	Clean Room Technology and Maintenance	DEC	3 – 0– 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Specify cleanroom standards and ancillary cleanrooms.
CO2	Identify fabrication materials and surface finishes.
CO3	Analyze air quantities, pressure differences and clean room disciplines

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1			3							1
CO2	1	1		3								
CO3			2									1

Detailed syllabus

Introduction, Cleanroom Classification Standards, Unidirectional air flow clean room, Basis of Clean room standards, Federal Standards 209 ,ISO standard 14644-1:1999,Cleanroom classification(Pharmaceutical, cleanrooms)

Design of Turbulently Ventilated and Ancillary Cleanrooms, Mini environments, isolators and RABS, Containment zone, Construction and clean build, Design of Unidirectional Cleanrooms.

High Efficiency Air filtration, Particle removal mechanisms, testing of high efficiency filters.

Cleanroom Testing and Monitoring, Principles of cleanroom testing, Testing in relation to room type and occupation state, Monitoring of cleanroom.

Measurement of Air Quantities and Pressure Differences, Air movement control, Recovery test methods, Cleanroom containment leak testing.

Filter Installation leak testing, Operating a clean room, Materials, equipment and machinery, Clothing, masks and gloves, Cleaning a cleanroom.

Reading:

1. William White, Cleanroom Technology: Fundamentals of Design, Testing and Operation, 2nd Edition, Wiley, 2010.
2. Matts Ramstorp, Introduction to Contamination Control and Cleanroom Technology, Wiley, 2008.
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000

EC5213	ULSI Technology	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand transmission electron microscopy.
CO2	Apply the concept of Metallization, interconnects, Process integration.
CO3	Understand fabrication issues of ULSI devices

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1		1	1	1						1
CO2	1	1										1
CO3	2	2		1		1						

Detailed syllabus

Microelectronics and microscopy, ULSI process technology, Application of TEM for construction analysis, TEM sample preparation techniques.

Ion implantation and substrate defects, Dielectrics and isolation, Silicides, polycide and salicide, Metallization and interconnects.

TEM in failure analysis, Novel devices and materials, TEM in under bump metallization and advanced electronics packaging technologies, High – resolution TEM in microelectronics.

ULSI devices I: DRAM cell with planar capacitor, ULSI devices II: DRAM cell with stacked capacitor, ULSI devices III: DRAM cell with trench capacitor, ULSI devices IV: SRAM.

Reading:

1. C. Y. Chang, S.M. Sze, ULSI Technology, McGraw-Hill, 2000.

2.Chih-Hang Tung, George T.T. Sheng, Chih-Yuan Lu, ULSI Semiconductor Process Technology Atlas, John Wiley & Sons, 2003.

EC5214	VLSI DSP ARCHITECTURES	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify and characterize the special architectural issues for DSP
CO2	Design efficient architectures & algorithms for improving speed and power consumption.
CO3	Translate effective algorithm design to integrated circuit implementations.
C04	Identify and minimize errors encountered during implementation of DSP algorithms

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1	1	2	1						1
CO2	2	2	1	3	3	1	1					1
CO3	2	1		2	2							
CO4	3	1		2	2							2

Detailed syllabus

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for Implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance: Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls.

Data path and control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls.

Enhancing performance with pipelining: An overview of pipelining, a pipe lined data path, pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards, using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

Computational accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, and DSP computational errors, D /A conversion errors.

Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Reading:

1. D.A, Patterson and J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier, 2011.
2. Avatar sigh, Srinivasan S, Digital signal processing implementations using DSP microprocessors with examples, Thomson 4th reprint, 2004.
3. Keshab Parhi, VLSI digital signal processing systems design and implementations, Wiley 1999

EC5215	Hardware / Software Co-Design	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify the need for co-design
CO2	Model data flow and implement the same through software and hardware
CO3	Construct data flow and control flow graphs
CO4	Design data flow model for a FSM
C05	Design an SoC for given application

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			1				2					1
CO2						1						
CO3	1	1					3					1
CO4			2			1						
CO5		1					1					

Detailed syllabus

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design. Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph4.4 Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph.

Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor

System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

Reading:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.
2. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

EC5216	Hardware Description Languages	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Differentiate sequential and concurrent languages
CO2	Design combinational logic circuits using HDL.
CO3	Design sequential logic circuits using HDL.
CO4	Model Analog circuits using Verilog AMS.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		2	2	1	2							1
CO2	1	1	1	1	3							1
CO3	1	1	1	1	2							
CO4	2	2	2	1	1							1

Detailed syllabus

Introduction: About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator overloading

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to One Hot

Introduction to Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling. Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior

Reading:

1.Volnei A. Pedroni, Circuit Design and Simulation with VHDL, 2nd Edition, MIT Press, 2010.

2. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004

EC5204	ANALOG IC DESIGN LAB	PCC	0 – 0 – 6	4 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Apply voltage and current biasing styles to design single stage amplifier.
CO2	Design and evaluate basic analog building blocks including sources, sinks, and mirrors, up to layout level.
CO3	Design an OP amp with pole splitting technique and measure the performance.
CO4	Design and test class-A and class-B output stages for OP amp.
CO5	Design optimally compensated OP amp upto tape-out considering parasitic effects.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	0	3	0	0	2	0	0	2			2
CO2	2	0	2	0	0	2						
CO3	1	1	2			2			1			2
CO4	1		2			1				2		1
CO5	1	1	3			3					2	2

Detailed syllabus

Cycle 1:

Lambda calculation for PMOS & NMOS, F_T calculation, Tranconductance plots, Single transistor amplifier, Ideal current source, PMOS current source, NMOS saturated load, Degenerative resistor, Cascade amplifier: Ideal current source, PMOS current source.

Cycle 2:

Current sinks: Basic current sink, Current sink with negative feedback, Bootstrap current sink, Cascode current sink, Regulated cascode current sink.

Current sources: Basic current source, Current source with negative feedback, Bootstrap current source, Cascade current source, Regulated cascade current source,

Current mirrors: Basic current mirror, Wilson current mirror, Cascode current mirror, Regulated cascade current mirror, Widlar current source

Differential amplifier, two stage Operational amplifier design

Reading:

1) Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2) Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3) Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

EC5205	Digital IC Design Laboratory	PCC	0 – 0 – 3	2 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Design synchronous and Asynchronous sequential circuits using Verilog HDL.
CO2	Develop soft methods for identifying faulty digital circuits for the DUT
CO3	Synthesize digital circuit using HDL.
CO4	Design combinational and sequential circuits at circuit level using Tanner tools
CO5	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits using EDA tool.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1		1	2	1			2			1
CO2	2	1		2	1	1		3	2			1
CO3											2	
CO4	1			2	3	2						1
CO5	1	1		3	1	1			2	2		1

Detailed Syllabus:

Module 1: CMOS inverters -static and dynamic characteristics, CMOS NAND, NOR and XOR Gates

Module 2: Static and Dynamic CMOS design- Domino and NORA logic – combinational and sequential circuits, Method of Logical Effort for transistor sizing –power consumption in CMOS gates- Low power CMOS design

Module 3: Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter –CMOS memory design - SRAM and DRAM

Module 4: Bipolar gate Design- BiCMOS logic - static and dynamic behavior –Delay and power consumption in BiCMOS Logic.

Module 5: Design and simulation of 32 bits MIPS processor

Reading:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.

2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

EC5251	Testing and Testability	PCC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same.
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	2	2	1			2				1
CO2	1	3	1	2	2		1	2				
CO3	2	2	1	2	2		1	2				2
CO4	1	1	1	1	2	2	1	3				
CO5	1	1	1	2	2	2		3				2

Detailed syllabus

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models

Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods

Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Reading:

1 M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.

Reference Books:

1. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002
2. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing forDigital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000
3. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989.

EC5252	Mixed Signal Design	PCC	4 – 0– 0	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Should be able to demonstrate corresponding layout techniques with least interference among digital and analog subsystems.
CO2	Should be in a position to design basic cells like OpAmp compensated and high ting against process and temperature variations meeting the mixed signal specifications
CO3	Should be able to design comparators that can meet the high speed requirements of digital circuitry.
C04	Should be able to design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching and phase noise, jitter.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1		1							1
CO2	1	1	3		1							3
CO3	1	1	3		3							3
CO4	1		3		2							

Detailed syllabus

Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower, Source-Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage Process and temperature independent compensation, Ahuza's compensation, nested miller compensation, dynamic offset cancellation techniques. Basic Building Blocks, OpAmp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator , Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit

Performance of Sample-and-Hold Circuits, Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and BiCMOS Sample-and-Holds, Translinear Gain Cell, Translinear Multiplier, Comparator Specifications Input Offset and Noise , Hysteresis, ,Using an OpAmp for a Comparator, Input-Offset Voltage Errors, Charge-Injection Errors, Making Charge-Injection Signal Independent , Minimizing Errors Due to Charge-Injection, speed of Multi-Stage Comparators, Latched Comparators, Latch-Mode Time Constant, Latch Offset, Examples of CMOS and BiCMOS Comparators, Input-Transistor Charge Trapping, Examples of Bipolar Comparators,

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters Multi-Bit Successive-Approximatio**n,** Algorithmic (or Cyclic) A/D Converter, Ratio-Independent Algorithmic Converter, Pipelined A/D Converters, One-Bit-Per-Stage Pipelined Converter,1.5 Bit Per Stage Pipelined Converter, Pipelined Converter Circuits,

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL Design Example, Jitter and Phase Noise, Period Jitter , P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , LC Oscillators , phase Noise of Oscillators, jitter and Phase Noise in PLLS

Reading:

1) David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2) R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986
3) Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008

EC5253	RF IC Design	PCC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the design bottlenecks specific to RF IC design
CO2	Identify noise sources, develop noise models for the devices and systems
CO3	Specify noise and interference performance metrics including noise figure, IIP3 and matching criteria.
C04	Characterize different multiple access techniques, wireless standards and various transceiver architectures
CO5	Design constituent blocks of RF receiver front end.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3		1			1				3
CO2	2		2		1	1						2
CO3	1		3		2	1		1				1
CO4			1		1							3
CO5	1		2		3							

Detailed syllabus

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology. BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

MULTIPLE ACCESS: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

AMPLIFIERS, MIXERS AND OSCILLATORS: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

POWER AMPLIFIERS: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

Reading:

1) Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001
2) Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.

EC5261	FPGA Design	DEC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand digital system design styles.
CO2	Implement memories, multipliers, shifters, ALU using PLD.
CO3	Synthesize special purpose processor using Vertex, Spartan FPGA cores.
C04	Design digital subsystems using parameterized library cells.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	2	1	1							2
CO2	2	1	2	3	3							1
CO3	2	1	2	3	2	1	1	1				2
CO4	3	1	1	2	2							

Detailed syllabus

INTRODUCTION TO FPGAs: Design and implementation of FPGA, Evolution of programmable devices, Application of FPGA.

DEISGN EXAMPLES USING PLDs Design of Universal block, Memory, Floating point multiplier, Barrel shifter.

SPECIAL PURPOSE PROCESSORS Programming technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FLEX 10k.

LOGIC BLOCK ARCHITECTURES

Logic block functionality versus area-efficiency, Logic block area and routing model, Impact of logic block functionality on FPGA performance, Model for measuring delay.

CASE STUDY – ACTEL FPGA

Reading:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.

2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

3. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.

EC5262	Full Custom Design	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand efficient Layout design techniques
CO2	Develop efficient layout techniques to absorb process variations.
CO3	Construct guard rings, pad rings suiting mixed signal environment
C04	Design layouts to minimize stress effects.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	1	3	3					
CO2		1		1		2	3	1				1
CO3	1		2	1	1	3	3	1				1
CO4		1	1	1		3	3	1				1

Detailed syllabus

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows**.**

Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals and Interconnect routing.

Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

Proper layout

CAD tools for layout, Planning tools, Layout generation tools, Support tools.

Reading:

1. Dan Clein, CMOS IC Layout Concepts Methodologies and Tools, Newnes, 2000.
2. Ray Alan Hastings, The Art of Analog Layout, 2nd Edition, Prentice Hall, 2006

EC5263	ASIC Design	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Architect ASIC library design
CO2	Develop programmable ASIC logic cells
CO3	Design I/O cells and interconnects
C04	Identify new developments in SOC and low power design.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		2			3	1						1
CO2				2	1	1						1
CO3	1	1			1	2						
CO4		2		3	1	1						1

Detailed syllabus

Introduction, Types of ASIC's Design Flow, CMOS Logic**.** ASIC Library Design, Transistor Parasitic Capacitance, Input Slew Rate, Library-Cell Design, Library Architecture. Programmable ASICs, The Antifuse Metal Antifuse, Static RAM, EPROM and EEPROM Technology, Practical Issues.

Programmable ASIC Logic Cells, Actel, Xilinx LCA., XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis, Logic Expanders. Programmable ASIC I/O Cells, Totem-Pole Output, Mixed-Voltage Systems, Metastability, Xilinx I/O Block. Boundary Scan.

Programmable ASIC Interconnect and Programmable ASIC Design Software. Actel ACT, RC Delay in Antifuse Connections, Xilinx EPLD Logic Synthesis, FPGA Synthesis, Third-party Software, low level design entry, logic synthesis, simulation,

Test and ASIC construction, VHDL, Verilog HDL, Logic Synthesis, Simulation.

Reading:

1. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.
2. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, 2nd Edition, Kluwer Academic, 2001.

EC 5264	Low Power VLSI Design	DEC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Identify sources of power consumption in a given VLSI Circuit
CO2	Analyze and estimate dynamic and leakage power components in a DSM VLSI circuit
CO3	Choose different types of SRAMs/ DRAMs for Low power applications
CO4	Design low power arithmetic circuits and systems
CO5	Estimate power consumption at different levels of abstraction in a VLSI system.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1		1	1							
CO2	1	1		1	2							
CO3		2		2	3							
CO4				3								
CO5				1								

Detailed syllabus

Introduction, Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation Designing for Low Power, Circuit Techniques for Leakage Power Reduction

Standard Adder Cells, CMOS Adders Architectures, Low Voltage Low Power Design Techniques, Current Mode Adders

Types of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques

The increased delays of wires, new materials for wires and dielectrics, Design methods taking into account interconnection delays, Cross talk

Basic background on testing, Unsuitable design techniques for safety-critical applications, Low power and safely operating circuits, Case study – A Low power subsystem design

Reading:

1. Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Edition 2009, Tata Mc Graw Hill
2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002
3. Jan Rabaey, Low Power Design Essentials, Springer.

EC5265	GaAs Technology	DEC	3 – 0 – 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify clearly the sources of power consumption in a given VLSI Circuit
CO2	Analyse and estimate dynamic and leakage power components in a DSM VLSI circuit
CO3	Choose different types of SRAMs/ DRAMs for Low power applications
CO4	Design low power arithmetic circuits and systems

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1		1								
CO2	1	1		2								1
CO3	2	1										
CO4	1	3		1								1

Detailed syllabus

Non-Silicon MOSFET Technology: Introduction, Brief and Non-Comprehensive History of the NSMOSFET, Surface Fermi Level Pinning: The Bane of NSMOSFET, Technology Development

Properties and Trade-Offs of Compound Semiconductor MOSFETs: Simulation Framework, Power-Performance Trade-offs in Binary III-V Materials (GaAs, InAs, InP and InSb) vs. Si and Ge, Power-Performance of Strained Ternary III-V Material (Inx Ga1−xAs), Strained III-V for p-MOSFETs. Device Physics and Performance Potential of III-VField-Effect Transistors: InGaAs HEMTs

Theory of Hfo2-Based High-K Dielectric Gate Stacks: Methodology of DFT Simulations of High-k Oxides on Semiconductor Substrates, DFT Simulations of High-k Oxides on Si/Ge Substrates.

Materials and Technologies for III-V MOSFETs: Introduction, III-V HEMTs for Digital Applications, Challenges for III-V MOSFETs, and Mobility in Buried Quantum Well Channel.

Atomic-Layer Deposited High-k/III-V Metal-Oxide-Semiconductor Devices and Correlated Empirical Model: History and Current, Empirical Model for III-V MOS, Experiments on High-k/III-V MOSFETs, Technology/Circuit Co-Design for III-V FETs.
Electrical and Material Characteristics of Hafnium Oxide with Silicon Interface Passivation on III-V Substrate for Future Scaled CMOS Technology: Introduction, MOSCAPs and MOSFETs on GaAs with Si, SiGe Interface Passivation Layer (IPL), MOSCAPs and MOSFETs on InGaAs with Si IPL, MOSCAPs and Self-Aligned n-channel MOSFETs on InP, Channel Materials with Si IPL.

Reading:

1. Serge Oktyabrsky, Peide D. Ye, Fundamentals of III-V Semiconductor MOSFETs, Springer, 2010.
2. C.Y. Chang, Francis Kai, GaAs High-speed Devices, Physics Technology and Circuit Applications, John Wiley, 1994.

EC 5266	Formal Verification	DEC	3 – 0 – 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Specify the formal verification techniques
CO2	Implement formal test plan process
CO3	Implement simulation based verification
CO4	Model hardware interfaces with concurrency constructs
CO5	Apply IEEE 1850 property specification language and IEEE1800 Verilog assertions

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2			1		3						1
CO2	1			1		2						
CO3	3		1			3						
CO4	1					3						1
CO5		1		1								

Detailed syllabus

Verification process: Verification plan, Debug Cycle, Simulation and Output data, Test bench development

Current verification techniques: HDL Software simulator, Accelerated simulation, Process Based Accelerator techniques, Hardware emulation, FPGA prototyping

Introduction to formal techniques and property specification: Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process

Techniques for proving properties: Abstraction reduction, Compositional reasoning, Counter abstraction, Gradual Exhaustive formal verification

Final system simulation: Module verification, Full simulation from a simulation, Full Simulation from a formal verification

IEEE 1850 PSL Property specifications and IEEE 1800 Verilog assertions: Introduction, operations and keywords, PSL Boolean and temporal layer, Introduction to IEEE 1800 System Verilog, Sequence and property, BNF 185 and BNF 223

Reading:

1. Douglas L Perry Harry D Foster, Applied Formal Verification, McGraw Hill, 2005.
2. William K Lam, Hardware Design Verification: Simulation and Formal Method-based Approaches, Prentice Hall, 2008.

EC5267	CAD for VLSI	DEC	3 – 0 – 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand steps involved in physical design automation
CO2	Identify algorithms required for circuit simulators
CO3	Incorporate timing analysis for floor planning
CO4	Apply scripting language PERL to improve EDA tool flow

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2					2	2					
CO2	1					2	3					1
CO3	1					3	1					1
CO4	1	1				2	1					

Detailed syllabus

Introduction to Design Methodologies: The VLSI Design Problem, Design Methods and Technologies, Layout Methodologies, Top-Down Approach: Routing: Fundamentals, Global Routing, Detailed Routing.

Performance Issues in Circuit Layout: Delay Models, Timing Driven Placement, Timing Driven Routing, Power Minimization.

Single-Layer Routing and Applications: Planar Subset Problem, Single-Layer Global Routing, Over-the-cell Routing, Multichip Modules, Wire-Length and Bend Minimization Techniques.

Reading:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2006.

2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.

EC 5268	MEMS and Microsystems	DEC	3 – 0 – 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the products and materials used in MEMS and Micro sensors.
CO2	Use the reconfigurable design implementation in MEMS.
CO3	Apply MEMs for bio medical applications

Mapping of course outcomes with program outcomes

C O	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	1	1	1							1
CO2		1	1	2	3	1						1
CO3	1	1		2	1							1

Detailed syllabus

OVERVIEW OF MEMS AND MICROSYSTEMS: Mems And Microsystems, Evolution of microfabrication, Microsystems and miniaturization, Application of Microsystems, Markets for Microsystems

WORKING PRINCIPLES OF MICROSYSTEMS: Introduction, MEMS and Micro actuators, Microfluidics, Micro actuators with Mechanical inertia

ENGINEERING SCIENCE FOR MICROSYSTEMS DESIGN: Introduction, Molecular theory of matter and intermolecular forces, Doping of semiconductor, Plasma physics, Electrochemistry

THERMOFLUID ENGINEERING AND MICROSYSTEMS DESIGN: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization

DESIGNING ARITHMETIC BUILDING BLOCKS: Introduction, Basic equation in continuum fluid dynamics, Laminar fluid flow in circular conduits, Computational fluid dynamics, incompressible fluid flow in micro-conduits

MICROSYSTEMS FABRICATION PROCESSES: Introduction, Photolithography, Diffusion, Oxidation, Chemical vapour deposition

Reading:

1. Tai-Ran Hsu, MEMS and Microsystems, 2nd Edition, Wiley, 2008.

2. Mohamad Gad El Hak, MEMS Design and Fabrication, 2nd Edition, CRC Press, 2006.

EC5269	Physical Design Automation	DEC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the complexity of physical design automation.
CO2	Identify algorithms suitable for partitioning a system.
CO3	Choose layout optimization techniques and translate them to the algorithms
CO4	Develop algorithms for local and global routing.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1			1	1	3	2					1
CO2	2			1		2	3					
CO3	1			1		3	2					1
CO4	1				1	2	2					1

Detailed syllabus

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules.

Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations,

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

Reading:

1) 1NaveedShervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2) Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

EC5254	MIXED SIGNAL DESIGN LAB	PCC	0 – 0 – 6	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Implement discrete- time signal processing circuits.
CO2	Implement layout techniques specific to mixed signal IC design.
CO3	Design OPamp for mixed signal environment.
CO4	Design a high speed comparator with high resolving capability.
CO5	Design data converters and RF circuits for mixed signal environment.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	3	1	1	2			2		2	1
CO2		1	3	1		3			2			1
CO3			2	1	1	1			2			1
CO4		1	2	1		1			2	2		1
CO5	1	1	3			2			2		2	1

Detailed Syllabus:

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
    i. Two stage cross coupled clamped comparator
    ii. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
    i. Parasitic sensitive integrator
    ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

Reading:

1) David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2) R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
3) Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4) Alan Hastlings, The art of Analog Layout, Wiley, 2005.

EC5255	Physical Design Automation Lab	PCC	0 – 0 – 6	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Apply the constraints posed by the VLSI fabrication technology to design automation tools using graph algorithms
CO2	Simulate partitioning algorithms viz., KL algorithm and simulated annealing algorithms.
CO3	Optimize floor planning using time driven floor planning algorithm and hierarchical tree based methods
CO4	Optimize routing using two terminal and multi terminal algorithms.

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		2					3			2		1
CO2	1	1			1	1	2	1	2		2	2
CO3		1			1	3	3	1	2			2
CO4	1	1	1	1		3	2	1	2	2		2

Detailed syllabus:

Cycle 1:

I. Depth first search
II. Breadth first search
III. Spanning tree algorithm
IV. Kruskal's algorithm
V. Dijkstra algorithm
VI. Floyd- Warshall algorithm

Cycle 2: Partitioning algorithms

a) Kernighan –Lin algorithm

b) Simulated annealing and evolution algorithms

Cycle 3 **Floor planning algorithms**

i) Constraint based methods

ii) Integer programming based methods

iii) Rectangular dualization based methods

iv) Hierarchical tree based methods

v) Simulated evolution algorithms

vi) Time driven Floorplanning algorithms

Cycle 4) Routing algorithms

I) Two terminal algorithms

a) Maze routing algorithms

b) Shortest path based algorithm

II) Multi terminal algorithm

i) SMST algorithm

ii) Z-RST algorithm

Reading:

1) NaveedShervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic, 1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.