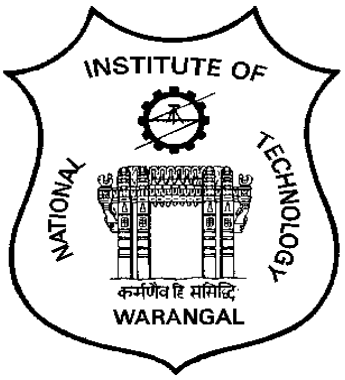
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL



SCHEME OF INSTRUCTION AND SYLLABI
FOR M.TECH PROGRAMS

Effective from 2019-20

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

VISION

Towards a Global Knowledge Hub, striving continuously in pursuit of excellence in Education, Research, Entrepreneurship and Technological services to the society

MISSION

- Imparting total quality education to develop innovative, entrepreneurial and ethical future professionals fit for globally competitive environment.
- Allowing stake holders to share our reservoir of experience in education and knowledge for mutual enrichment in the field of technical education.
- Fostering product oriented research for establishing a self-sustaining and wealth creating centre to serve the societal needs.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Create an Educational environment to prepare the students to meet the challenges of modern electronics and communication Industry through state of art technical knowledge and innovative approaches.

MISSION

- To create learning, development and testing environment to meet ever challenging needs of the Electronic Industry.
- To create entrepreneurial environment and industry interaction for mutual benefit.
- To be a global partner in training human resources in the field of chip design, instrumentation and networking.
- To associate with international reputed institution for academic excellence and collaborative research.

MASTER OF TECHNOLOGY

ELECTRONICS AND COMMUNICATION ENGINEERING

SPECIALIZATION: VLSI SYSTEM DESIGN

SCHEME AND SYLLABI

COURSE CURRICULUM FOR THE M.TECH PROGRAMME IN

VLSI SYSTEM DESIGN

Program Education Objectives

PEO 1	Design and generate GDS files for digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, algorithms and develop testing methods.
PEO 2	Model passive and active devices suiting advances in IC fabrication technology.
PEO 3	Design low power and improved performance VLSI signal processing architectures and implement them on FPGA platforms.
PEO 4	Communicate effectively and convey ideas using innovative engineering tools.
PEO 5	Perceive lifelong learning as a means of enhancing knowledge base and skills necessary to contribute to the improvement of their profession and community.

PEO-Mission matrix

Mission	PEO1	PEO2	PEO3	PE04	PEO5
• To create learning, development and testing environment to meet ever challenging needs of the Electronic industry.	3	3	3	2	2
• To create entrepreneurial environment and industry interaction for mutual benefit.	2	2	2	3	3
• To be a global partner in Training the human resource in the fields of Chip Design, Instrumentation and Networking.	2	3	2	2	3
• To associate with internationally reputed Institutions for academic excellence and collaborative research.	2	2	2	2	3

Graduate Attributes

These Graduate Attributes are identified by National Board of Accreditation.

1. Scholarship of Knowledge: Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

2. Critical Thinking: Analyze complex engineering problems critically, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

3. Problem Solving: Think laterally and originally, conceptualize and solve engineering problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

4. Research Skill: Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

5. Usage of modern tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

6. Collaborative and Multidisciplinary work: Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

7. Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economic and financial factors.

8. Communication: Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

9. Life-long Learning: Recognize the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

10. Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of

the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

11. Independent and Reflective Learning: Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.

Program Outcomes

PO1	Identify, characterize, model and offer solutions to issues related to IC design
PO2	Understand the advances in the VLSI technologies
PO3	Identify design requirements of analog and mixed signal circuits
PO4	Design low power digital integrated circuits
PO5	Develop efficient architectures for improving system performance in terms of speed, power consumption, and accuracy.
PO6	Perform all design functions using EDA tools.
PO7	Specify appropriate physical design automation algorithm meeting system requirements.
PO8	Develop test strategies suitable for the integrated circuits in analog and mixed signal domain.
PO9	Communicate technical material through formal written reports satisfying accepted standards of writing style while adopting professional ethics
PO10	Work in a team effectively with improved communication skills.
PO11	Understand how organizations work, generate wealth, manage finances and effectively utilize human resources.
PO12	Develop lifelong learning methods.

Mapping of POs and PEOs

	PEO1	PEO2	PEO3	PEO4	PEO5
PO1	3	3	2	1	2
PO2	2	3	2	1	2
PO3	3	2	2	1	2
PO4	2	2	3	1	2
PO5	2	2	3	1	2
PO6	3	1	1	1	2
PO7	3	1	2	1	2
PO8	3	3	1	1	2
PO9	1	1	1	3	2
PO10				3	2
PO11				3	
PO12	1	1	1	2	3

Scheme of Instruction and Evaluation

I Year I Semester

Sl. No.	Course Code	Course Title	L	T	P	Credits
1.	EC5201	Microchip Fabrication Techniques	3	0	0	3
2.	EC5202	Device Modeling	3	0	0	3
3.	EC5203	Digital IC Design	3	0	0	3
4.	EC5204	Analog IC Design	3	0	0	3
5.		Elective–I	3	0	0	3
6.		Elective-II	3	0	0	3
7.	EC5205	Analog IC Design Laboratory	0	0	3	2
8.	EC5206	Digital IC Design Laboratory	0	0	3	2
9.	EC5291	Seminar	0	0	2	1
Total						**23**

I Year II Semester

Sl. No.	Course Code	Course Title	L	T	P	Credits
1.	EC5251	Physical Design Automation	3	0	0	3
2.	EC5252	Mixed Signal Design	3	0	0	3
3.		Elective – III	3	0	0	3
4.		Elective – IV	3	0	0	3
5.		Elective – V	3	0	0	3
6.		Elective – VI	3	0	0	3
7.	EC5253	Mixed Signal Design Laboratory	0	0	3	2
8.	EC5254	Physical Design Automation Laboratory	0	0	3	2
9.	EC5292	Seminar	0	0	2	1
Total						**23**

II Year I Semester

S.No	Course No	Course name	Credits
1	EC6241	Comprehensive Viva	2
2	EC6249	Dissertation Part A	9
Total			**11**

II Year II Semester

S.No	Course No	Course name	Credits
1	EC6299	Dissertation Part B	18

Total No. of credits - 75

Credit Structure

Credits	Sem I	Sem II	Sem III	Sem IV	Range
CORE COURSES	**12**	**6**	00	00	**18**
Elective	**06**	**12**	00	00	**18**
Lab courses	**04**	**04**	00	00	**08**
Seminar	01	01	00	00	**02**
Comprehensive viva-voce	00	00	**02**	00	**02**
Project	00	00	**09**	**18**	**27**
Total credits	**23**	**23**	**11**	**18**	**75**

List of Electives

S.No	Course No	Course Title
Elective-I	EC5207	Nano-electronic Materials and Devices
	EC5208	MEMS and NEMS
	EC5209	Fundamentals of Nanoelectronics
Elective-II	EC5210	Low power VLSI Design
	EC5211	VLSI Architectures
	EC5212	Hardware Description Languages
Elective-III	EC5255	CMOS RF IC Design
	EC5256	Electronic Design Automation
	EC5257	CAD for VLSI
Elective-IV	EC5258	FPGA Design
	EC5259	Full Custom Design
	EC5260	ASIC System Design
Elective V	EC5261	Hardware/Software Co-design
	EC5262	VLSI Test and Testability
	EC5263	VLSI Design Verification
Elective-VI	EC5264	Embedded System and RTOS
	EC5265	Reliability of Devices and Circuits
	EC5266	Modern Computer Architecture

EC5201	Microchip Fabrication Techniques	Core	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Specify the unit fabrication process steps
CO2	Explain the process flow for MOS devices
CO3	Analyze process yield and yield measurement for a process

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2		1			1					1
CO2	1	1										1
CO3	1	1		1		1	1					

Detailed Syllabus:

Overview of semiconductor industry, unit process steps for fabrication, Process Flow for NMOS, PMOS, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.

Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping, Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

Process flow for CMOS, BICMOS ICs, and Novel MOS devices
Packaging: Chip characteristics, package functions, package operations

Text books:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.
3. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
5. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

EC5202	Device Modeling	Core	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Develop mathematical models for modern MOS devices.
CO2	Develop solution to overcome short channel issues.
CO3	Develop various compact models appropriate for industry.
CO4	Analyse current distribution in the devices like transistors, MOS devices.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	1	1	3						3
CO2	2	3	1	1	1	2						2
CO3	2	3	2	2	1	1						3
CO4	1	2	1	1	1	1						3

Detailed Syllabus: (Semiconductor Device Modelling)

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

The MOS transistor: Small signal modelling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

The bipolar transistor: Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics

Compact Modeling: Compact model Level 1, Level 2, Level 3, UTB/FD SOI MOSFET, FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

Text books/ References:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.

2. M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017.

3. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.

4. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

5. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

EC5203	Digital IC Design	Core	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Design CMOS inverters with specified noise margin and propagation delay.
CO2	Synthesize digital circuit using Verilog HDL.
CO3	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits.
CO4	Design a processor meeting timing constraints.
CO5	Design memories with efficient architectures to improve access times, power consumption.

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	2	3	2							1
CO2	2	1	1	1	2	2	1					
CO3	2	1	1	2	3	1		1				1
CO4	1	1	2	2	2	1	2	1				
CO5	1	1	1	2	3			1				

Detailed Syllabus:

MOS INVERTERS: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations.

DESIGNING COMBINATIONAL & SEQUENTIAL LOGIC GATES in CMOS: Static CMOS Design, Dynamic CMOS Design, Power Consumption in CMOS Gates.
Static Sequential Circuits, Dynamic Sequential Circuits, Non-Bistable Sequential Circuits, Logic Style for Pipelined Structures.

TIMING ISSUES IN DIGITAL CIRCUITS: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization.

DESIGNING ARITHMETIC BUILDING BLOCKS: Introduction, The Adder: Definition, Circuit and Logic Design, The Multiplier: Definition, The Shifter: Definition, Power Considerations in Datapath Structures.

DESIGNING MEMORY: Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM, Memory Peripheral Circuitry, Embedded DRAM.

Advanced Digital IC Design: Block level design

Text Books:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.
2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

EC5204	ANALOG IC DESIGN	Core	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different circuits
CO2	Design all basic building blocks like sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and should be able to design OpAmp fully Compensated against process, supply and temperature variations.
CO4	Identify the suitable different topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.
CO5	Design Analog integrated system completely upto tape-out including parasitic effects.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3		2	1		1				3
CO2	2	1	3		2	2		1				2
CO3	2	1	3		2	1						
CO4	1	1	3		3	2						
CO5	1	1	3		2	1						2

Detailed Syllabus:

MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices.

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references.

Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, Cascode, folded cascode, choice of device models.

Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, replication principle, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion, gilbert cell

Operational amplifier-characterization, 2 stage OP amp, process and temperature independent compensation, output stage.

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, constant g_m biasing, speed and noise issues, case study, curvature correction.
PTAT, CTAT, Bandgap circuit, start-up circuit, curvature correction Design.

Negative feedback amplifier design with Nyquist criteria analysis.

Text Books:

1. Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

EC5207	Nano-electronic Devices and Materials	Elective - I	3-0-0	3 Credits

Prerequisites: Basic understanding of semiconductor devices.
Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the physics and materials for Nanoelectronics
CO2	Understand the scaling issues and need for non-classical devices
CO3	Analyse the performance of novel devices

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			1				2					1
CO2						1						
CO3	1	1					3					1

Detailed Syllabus:

Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore's Law and Koomey's law.
Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Metal gate transistor : Motivation, requirements, Integration Issues.

Non classical MOS transistor: Requirements, and Novel devices
SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues.
Vertical transistors - FinFET and Cylindrical gate FET.
Novel devices: Tunnel FET, Negative-Capacitance (NC) FET.
Metal source/drain junctions - Properties of schotky junctions on Silicon, Germanium and compound semiconductors -Workfunction pinning.
Germanium Nano MOSFETs : strain , quantization , Advantages of Germanium over Silicon, PMOS versus NMOS.
Compound semiconductors - Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs, exploiting novel materials, strain, quantization.

Emerging nano materials : CNT, Graphene, Nanotubes, nanorods and other nano-structures.

Text Books:

1. Y. Taur and T. Ning, "Fundamentals of Modern VLSI devices" Cambridge University Press
4. Nicollian and J. R. Brews "MOS (Metal Oxide Semiconductor) Physics and Technology" Wiley Publishers

5. Brundle, C.Richard; Evans, Charles A. Jr.; Wilson, Shaun “Encyclopedia of Materials Characterization”, Elsevier.
6. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017.
7. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009
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8. Related research papers.

EC5208	MEMS & NEMS	Elective - I	3-0-0	3 Credits

Prerequisites: Basics of VLSI Technology

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the micro-fabrication principles.
CO2	Design a MEMS capacitive switch.
CO3	Apply MEMS concepts for sensor and optical device design.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	1	1	1							1
CO2		1	1	2	3	1						1
CO3	1	1	2		1							1

Detailed Syllabus:

Introduction to Micro-fabrication: Cleaning, Oxidation, Diffusion, Mask making, Lithography, Etching, Ion Implantation, CVD, PVD, Metallization; Surface micromachining and Bulk Micromachining, DRIE, LIGA, Fabrication of high aspect ratio deformable structures

Elasticity in Materials: Stress, strain calculations, Normal and Shear strains and constitutive relations, Plane stress, biaxial stress, residual stress, energy relations, Load-deflection calculations in beams, cantilevers (rectangular cross section), Elastic deformation in square plate, Resonant frequency calculations: Rayleigh-Ritz method

MEMS Capacitive Switch: Lumped model, pull-in voltage, Electromechanical deflection modeling, pull-in instability, switching time and pull-in voltage scaling, Physical effects in nanoscale gap-size, squeeze-film damping , perforated MEMS Capacitive switch, Comb actuators, Accelerometer, Pressure sensor, Energy approach: Lagrangian Mechanics applicable to MEMS capacitive switches, Reliability in RF-capacitive switch

MEMS Sensors: Thermal sensor, Interaction of Thermal-Electrical Fields, Numerical design of thermal sensors, Bio-MEMS design problems

Optical MEMS: 2-D, 3-D switches, design examples.

Text Books:

1. Rebeiz, G.M., RF MEMS: Theory Design and Technology,Wiley 1999
2. Stephen D. Senturia, Microsystem Design, Kluwer Academic 2001
3. Madou, M., Fundamentals of Microfabrication, CRC Press 1997
4. Sandana A., Engineering biosensors: kinetics and design applications, Academic Press 2002
5. Related research papers

EC5209	Fundamentals of Nanoelectronics	Elective - I	3-0-0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the concept of electrical and thermal conductivity in metal
CO2	Understand the crystal structure and bravais lattice types
CO3	Study the concept of energy band gaps and Tight Binding Model
CO4	Analyse the Ferromagnetism in solids

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			1				2					1
CO2						1						
CO3	1	1					3					1
CO4			2			1						
CO5		1					1					

Detailed Syllabus:

Drude's model: Introduction to Drude's theory of electrons in a metal, Postulates of Drude's theory, Calculating electrical conductivity of metal using Drude's Model, Hall effect in metals, Understanding thermal conductivity of a metal using Drude's model

Sommerfeld's model: Fermi energy and Fermi Sphere, Density of states; Specific heat of an electron gas and the behaviour of thermal conductivity of a solid and relationship with electrical conductivity; Introduction to magnetism in metal

Crystal structure and their classifications: Understanding crystal structure using Bravais Lattice, Bravais lattice types, different crystal types, indexing crystal planes

Vibrations of crystals with monoatomic basis, Acoustic and optical modes; Two atoms ates, per primitive basis, Quantization of Elastic waves, Density of states of phonons, Phonon Momentum

Bloch's theorem for wavefunction of a particle in a periodic potential, Nearly free electron model, origin of energy band gaps; Kronig-penney Model, Tight Binding Model

Magnetism in materials; Superconductivity.

Text Books:

1. John Singleton, Band Theory and Electronic Properties of Solids, Oxford, 2001.
2. Prasanta K. Misra, Physics of Condensed Matter, Elsevier, 2012.
3. M. L. Cohen and S. G. Louie, Fundamentals of Condensed Matter Physics, Cambridge university Press, 2016.
4. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017.

EC5210	Low Power VLSI Design	Elective - II	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify clearly the sources of power consumption in a given VLSI Circuit.
CO2	Analyze and estimate dynamic and leakage power components in a DSM VLSI Circuit.
CO3	Choose the types of SRAMs/ DRAMs for the given Low power applications.
CO4	Design low power arithmetic circuits and systems.
CO5	Decide at which level of abstraction is advantageous to implement low power techniques in a VLSI system design.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1		1	1							
CO2	1	1		1	2							
CO3		2		2	3							1
CO4				3								1
CO5				1								

Topics Covered:

Introduction, Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation.
Designing for Low Power, Circuit Techniques for Leakage Power Reduction.

Standard Adder Cells, CMOS Adders Architectures, Low Voltage Low Power Design Techniques, Current Mode Adders.

Types of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison.

Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques, Embedded DRAM.

The increased delays of wires, New materials for wires and dielectrics, Design methods taking into account interconnection delays, Cross talk.

Basic background on testing, Unsuitable design techniques for safety-critical applications, Low power and safely operating circuits, Case study – A Low power subsystem design

Text Books:

1. Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Edition 2009, Tata Mc Graw Hill

2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002

Reference Book:

1. Jan Rabaey, Low Power Design Essentials, Springer.

EC5211	VLSI ARCHITECTURES	Elective II	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Design of RISC architecture and controller for a specific instruction set.
CO2	Improve the performance of RISC processor by employing pipelining.
CO3	Translate DSP algorithm into an efficient architecture and study the design of different building blocks of DSP architectures.
CO4	Estimate the effect of folding, unfolding and retiming techniques on the performance of DSP architectures.

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1	1	2	1						1
CO2	2	2	1	3	3	1	1					1
CO3	2	1		2	2							
CO4	3	1		2	2							2

Topics Covered:

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for Implementation as VLSI Chips, CPU performance and its factors, evaluating performance.

Design of RISC processor**,** Enhancing performance with pipelining**:** An overview of pipelining, pipelined implementation of RISC instruction set, various hazards of pipelining, Hazard free pipelined RISC implementation

Architectures for programmable digital signal processing devices: representation of DSP algorithms**,** basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Iterative bound: Introduction, data flow graph representations, loop bound and iterative bound, algorithms for computing iteration bound, iteration bound of multi rate data flow graphs.

Pipe lining and parallel processing: Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power

Retiming: Introduction, definitions and properties, retiming techniques.

Unfolding: Introduction, an algorithm for unfolding, properties of unfolding, critical path, unfolding, and retiming. Applications of unfolding.
Folding: Introduction, folding transformation, register minimization techniques.

Text Books:

1. D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier, 2011.
2. Keshab Parhi, VLSI digital signal processing systems design and implementations, Wiley 1999
3. Avatar sigh, Srinivasan S, Digital signal processing implementations using DSP microprocessors with examples, Thomson 4th reprint, 2004.

EC5212	Hardware Description Languages	Elective III	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Differentiate sequential language and concurrent language.
CO2	Design combinational logic circuits using VHDL.
CO3	Design sequential logic circuits using VHDL.
CO4	Model Analog circuits using Verilog AMS.
CO5	Differentiate sequential language and concurrent language.

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		2	2	1	2							1
CO2	1	1	1	1	3							1
CO3	1	1	1	1	2							
CO4	2	2	2	1	1							1

Detailed Syllabus:

Verilog: About Verilog, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading.

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits.

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot.

System Verilog: Verilog +, Coverage, Randomization, Assertion, functional coverage, Object oriented programming, define – parameter.

Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling.

Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior.

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003.
2. Chris Spear, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd ed., Springer, 2012
3. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004.

EC5205	ANALOG IC DESIGN LAB	Core	0-0-4	2 Credits

Prerequisites: Analog IC Design

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different Analog circuits.
CO2	Design all basic building blocks viz., sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and design OPamp fully compensated against process, supply and temperature variations.
CO4	Specify suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.
CO5	Design Analog integrated circuits taking account the parasitic effects.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2		3		2	2			2			2
CO2	2		2		2	2						
CO3	1	1	2		2	2			1			2
CO4	1		2		3	1				2		1
CO5	1	1	3		2	3					2	2

Detailed Syllabus:

Cycle 1:

Lambda calculation for PMOS & NMOS, F_T calculation, Transconductance plots, Single transistor amplifier, Ideal current source, PMOS current source, NMOS saturated load, Degenerative resistor, Cascade amplifier: Ideal current source, PMOS current source.

Cycle 2:

Current sinks: Basic current sink, Current sink with negative feedback, Bootstrap current sink, Cascode current sink, Regulated cascode current sink.

Current sources: Basic current source, Current source with negative feedback, Bootstrap current source, Cascade current source, Regulated cascade current source,

Current mirrors: Basic current mirror, Wilson current mirror, Cascode current mirror, Regulated cascade current mirror, Widlar current source

Differential amplifier, Two stage Operational amplifier design

Text Books:

1) Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2) Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3) Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

EC5206	Digital IC Design Laboratory	Core	0-0-4	2 Credits

Prerequisites: Digital IC Design

Course Outcomes: At the end of the course the student will be able to:

CO1	Design of combinational and sequential circuits using Verilog HDL/ VHDL
CO2	Synthesize digital circuit targeting state of the art FPGA
CO3	Design combinational and sequential circuits at circuit level using EDA tools
CO4	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits using EDA tools.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1		1	2	1			2			1
CO2	2	1		2	1	1		3	2			1
CO3											2	
CO4	2			2	3	2			2	2		1

Detailed Syllabus:

Module 1:

CMOS inverters -static and dynamic characteristics, CMOS NAND, NOR and XOR Gates. Static and Dynamic CMOS design- Domino and NORA logic – combinational and sequential circuits -Method of Logical Effort for transistor sizing –power consumption in CMOS gates- Low power CMOS design.

Module 2:

Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter –CMOS memory design - SRAM and DRAM.

Module 3:

Design and simulation of 16 or 32 bits MIPS processor

Module 4:

Mini Project

Text Books:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.
2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

EC5251	Physical Design Automation	Core	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Students should have understood the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
CO2	Should be able to adapt the design algorithms to meet the critical design parameters.
CO3	Should have learnt various layout optimization techniques and should be able to map them to the algorithms.
CO4	Should be in a position to develop proto-type EDA tool and test its efficacy.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1			1	1	3	2					1
CO2	2			1		2	3					
CO3	1			1		3	2					1
CO4	1				1	2	2					1

Detailed Syllabus:

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules.

Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Text Books:

1) Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2) Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

EC5252	Mixed Signal Design	Core	3-0-0	3 Credits

Prerequisites: Analog and Digital IC Design

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the necessity of mixed signal systems and demonstrate corresponding layout techniques with least interference among digital and analog subsystems.
CO2	Design basic cells like OpAmp to meet the mixed signal specifications.
CO3	Design comparators to meet the high speed requirements of digital circuitry.
CO4	Design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing jitter, switching and phase noise.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1		1							1
CO2	1	1	3		1							3
CO3	1	1	3		3							3
CO4	1		3		2							
CO5	1	2			2							2

Topics Covered:

Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower, Source-Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage

Process and temperature independent compensation, Ahuza's compensation, nested miller compensation, dynamic offset cancellation techniques.

Basic Building Blocks, OpAmp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator , Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit.

Performance of Sample-and-Hold Circuits, Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and BiCMOS Sample-and-Holds, Translinear Gain Cell, Translinear Multiplier

Comparator Specifications Input Offset and Noise , Hysteresis, ,Using an OpAmp for a Comparator, Input-Offset Voltage Errors, Charge-Injection Errors, Making Charge-Injection Signal Independent , Minimizing Errors Due to Charge-Injection, speed of Multi-Stage Comparators, Latched Comparators, Latch-Mode Time Constant, Latch Offset, Examples of CMOS and BiCMOS Comparators, Input-Transistor Charge Trapping, Examples of Bipolar Comparators,

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity

Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters.

Multi-Bit Successive-Approximatio**n,** Algorithmic (or Cyclic) A/D Converter, Ratio-Independent Algorithmic Converter, Pipelined A/D Converters, One-Bit-Per-Stage Pipelined Converter,1.5 Bit Per Stage Pipelined Converter, Pipelined Converter Circuits,

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL characterization and Design Example. Jitter and Phase Noise, Period Jitter , P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLS

Text Books:

1) David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2) R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986
3) Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008

EC5255	CMOS RF IC Design	Elective III	3-0-0	3 Credits

Prerequisites: Analog IC Design

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the design bottlenecks specific to RF IC design
CO2	Identify noise sources and develop noise models for the devices and systems.
CO3	Identify various techniques to improve the bandwidth of RF amplifiers.
CO4	Design various RF amplifiers

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3		1			1				3
CO2	2		2		1	1						2
CO3	1		3		2	1		1				3
CO4	1		2		3							

Basic concepts of RF IC design

Design Bottle necks of RF IC design Non linearity and Time invariance Sensitivity and dynamic range, Passive impedance transformation, RF radio receiver front end non idealities and design parameters: Effects of nonlinearity, 1 dB compression point, Derivation of required noise figure at receiver front end, Required IIP_3 at receiver front end, Partitioning of required NF at receiver front end and IIP_3 into individual NF and IIP_3.

Noise: Noise sources in MOSFETs, Modeling of thermal noise and flicker noise, noise analog integrated circuits.

Low Noise Amplifier: Introduction : General Philosophy, Matching Networks, Comparisions of Narrowband and wideband LNA.
Wideband LNA Design: DC Bias, Gain ad Frequency Response, Noise Figure.
Narrowband LNA: Impedance matching, Matching the imaginary part matching the real part, interpretation of power matching similarity between Q factor and turns ratio.
Narrowband LNA: Principles, Core amplifier design, noise figure, power dissipation, trade offs between noise figure and power dissipation, noise contribution from other sources.

Mixers: Active Mixer, modeling mixers, unbalanced mixer circuits, single balanced mixer circuit, double balanced mixer circuits, Quantitative description of Gilbert mixer, conversion gain, Distortion, analysis of Gilbert mixer. Passive mixers: Switchig mixer, distortion in in unbalanced switching mixer, conversion gain and noise.

Frequency synthesizer and Clock recovery circuits: PLL based frequency synthesizer: Concepts of PLL, phase detector, charge pump, RF Synthesizer architectures, Frequency Dividers, VCO, LC oscillators, Ring oscillator, Phase noise, Loop filter and system design.

TEXT BOOKS:

1. VLSI for wireless communication , Bosco Leung, PrenticeHall
2. RF Microelectronics by Behad Razavi , PrenticeHall

EC5256	Electronic Design Automation	Elective III	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	To learn a number of circuit analysis techniques such as nodal analysis, mesh analysis, modified nodal analysis and hybrid analysis.
CO2	To formulate equations and solve nonlinear networks.
CO3	To determine the convergence and stability boundary for multi-step or multi-stage methods applied to a linear system of ODEs.
CO4	To introduce special classes of multistep methods for the solution of electrical networks.
CO5	To introduce general purpose circuit simulators and learn the fundamental equations for semiconductor devices.
CO6	To understand the physical or empirical models of semiconductor parameters in small signal analysis

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3		1			1				3
CO2	2		2		1	1						2
CO3	1		3		2	1		1				1
CO4			1		1							3
CO5	1		2		3							
CO6												

Formulation of network equations: Nodal, mesh, modified nodal and hybrid analysis equations; Sparse matrix techniques; Solution of nonlinear networks through Newton-Raphson technique; Multistep methods: convergence and stability; Special classes of multistep methods: Adams-bashforth, Adams-Moulton and Gear's methods; Solution of stiff systems of equations; Adaptation of multistep methods to the solution of electrical networks; General purpose circuit simulators.

Review of semiconductor equations (Poisson, continuity, drift-diffusion, trap rate). Finite difference formulation of these equations in 1D and 2D. Grid generation; Physical/empirical models of semiconductor parameters (mobility, lifetime, band gap, etc.); Computation of characteristics of simple devices (p-n junction, MOS capacitor, MOSFET, etc.); Small-signal analysis.

TEXT BOOKS:

1. L.O. Chua and P.M. Lin, Computer aided analysis and electronic circuits, Prentice Hall, 1975.
2. S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer-Verlag, 1984.
3. N.J. McCalla, Fundamentals of Computer Aided Circuit Simulation, Kluwer Academic Publishers, 1988.

EC5257	CAD for VLSI	Elective II	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Specify layout techniques in IC.
CO2	Identify algorithms required for circuit simulators.
CO3	Incorporate timing analysis and floor planning.
CO4	Apply scripting language PERL to improve EDA tool flow.
CO5	Specify layout techniques in IC.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2					2	2					
CO2	1	1				2	3					1
CO3	1					3	1					1
CO4	1	1				2	1					

Detailed Syllabus:

Introduction to Design Methodologies: The VLSI Design Problem, Design Methods and Technologies, Layout Methodologies, Top-Down Approach: Routing: Fundamentals, Global Routing, Detailed Routing.

Performance Issues in Circuit Layout: Delay Models, Timing Driven Placement, Timing Driven Routing, Power Minimization.

Single-Layer Routing and Applications: Planar Subset Problem, Single-Layer Global Routing, Over-the-cell Routing, Multichip Modules, Wire-Length and Bend Minimization Techniques.

Cell Generation and Programmable Structures: Programmable Logic Arrays, Transistor Chaining, Weinberger Arrays and Gate Matrix Layout, CMOS Cell Layout Styles Considering Performance Issues, Compaction: 1D Compaction, 2D Compaction.

Text Books:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2006.
2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.

EC5258	FPGA Design	Elective-IV	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand FPGA design flow.
CO2	Identify the building blocks of commercially available FPGA/CPLDs.
CO3	Develop VHDL/Verilog models and synthesize targeting for Vertex, Spartan FPGAs.
CO4	Develop parameterized library cells and implement system designs using parameterized cells.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	2	1	1							2
CO2	2	1	2	3	3							1
CO3	2	1	2	3	2	1	1	1				2
CO4	3		1	2	2							

Topics Covered:

INTRODUCTION TO FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.

DEISGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter.

FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA

CASE STUDY – Applications using Kintex-7, Viretex-7, Artix-7.

Text Books:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.

2. Data sheets of Artix-7, Kintex-7, Virtex-7 .

3. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

EC5259	Full Custom Design	Elective IV	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand efficient Layout design techniques.
CO2	Absorb the process variations into the layout.
CO3	Construct guard rings, pad rings suiting mixed signal environment.
CO4	Design layouts minimizing stress effects.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	1	3	3					
CO2		1		1		2	3	1				1
CO3	1		2	1	1	3	3	1				1
CO4		1	1	1		3	3	1				

Topics Covered:

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

Advanced techniques for specialized building blocks: Standard cell libraries, Pad cells and Laser fuse cells, advanced techniques for building blocks, Power grid Clock signals and Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

Layout considerations due to process constraints: Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings , Constructing the pad ring , Minimizing Stress effects.

Proper layout: CAD tools for layout, planning tools, Layout generation tools, Support tools.

Text Books:

1. Dan Clein, CMOS IC Layout Concepts Methodologies and Tools, Newnes, 2000.
2. Ray Alan Hastings, The Art of Analog Layout, 2nd Edition, Prentice Hall, 2006

EC5260	ASIC System Design	Elective - IV	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Architect ASIC library design.
CO2	Develop programmable ASIC logic cells.
CO3	Design I/O cells and interconnects.
CO4	Identification of new developments in SOC and low power design.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		2			3	1						1
CO2				2	1	1						1
CO3	1	1			1	2						
CO4		2		3	1	1						1

Topics Covered:

Introduction : Types of ASIC's, Design Flow , CMOS Logic.

ASIC Library Design: Transistor Parasitic Capacitance, Input Slew Rate, Library-Cell Design, Library Architecture.

Programmable ASICs: The Antifuse, Metal Antifuse, Static RAM ,EPROM and EEPROM Technology ,Practical Issues.

Programmable ASIC Logic Cells: Actel, Xilinx LCA, XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis, Logic Expanders.

Programmable ASIC I/O Cells: Totem-Pole Output, Mixed-Voltage Systems, Metastability, Xilinx I/O Block, Boundary Scan.

Programmable ASIC Interconnect and Programmable ASIC Design Software:
Actel ACT, RC Delay in Antifuse Connections, Xilinx EPLD, Logic Synthesis, FPGA Synthesis, Third-party Software.

Low Level Design Entry, Logic Synthesis, Simulation, Test And ASIC Construction:
VHDL, Verilog HDL, Logic Synthesis, Simulation.

Text Books:

1. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.
2. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, 2nd Edition, Kluwer Academic, 2001.

EC5261	Hardware / Software Co-Design	Elective V	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand Serial and parallel communication protocols.
CO2	Model data flow and implement the same through software and hardware.
CO3	Operate data flow using USB and CAN bus for PIC microcontrollers.
CO4	Design embedded Ethernet for Rabbit processors.
CO5	Design CORDIC and Crypto coprocessor.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			1				2					1
CO2						1						
CO3	1	1					3					1
CO4			2			1						
CO5		1					1					

Detailed Syllabus:

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design.

Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph4.4 Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph.

Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor.

System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

Text Books:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.
2. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

EC5262	VLSI Test and Testability	Elective - V	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same.
CO3	Specify fabrication defects, errors and faults
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	2	2	1			2				1
CO2	1	3	1	2	2		1	2				
CO3	2	2	1	2	2		1	2				2
CO4	1	1	1	1	2	2	1	3				
CO5	1	1	1	2	2	2		3				2

Topics Covered:

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.

Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.

Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method.

D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches Test pattern generation for BIST, Circular BIST. BIST Architectures. Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Text Books:

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.

Reference Books:

1. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002
2. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000.
3. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

EC5263	VLSI Design Verification	Elective V	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Specify the formal verification techniques.
CO2	Implement formal test plan process.
CO3	Implement simulation based verification.
CO4	Model hardware interfaces with concurrency constructs.
CO5	Apply IEEE 1850 property specification language and IEEE1800 Verilog assertions.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2			1		3						1
CO2	1			1		2						
CO3	3		1			3						1
CO4	1					3						1
CO5		1		1								

Detailed Syllabus:

Verification process: Verification plan, Debug Cycle, Simulation and Output data, Testbench development.

Current verification techniques: HDL Software simulator, Accelerated simulation, Process-Based Accelerator techniques, Hardware emulation, FPGA prototyping.

Introduction to formal techniques and property specification: Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process.

Techniques for proving properties: Abstraction reduction, Compositional reasoning, Counter abstraction, Gradual Exhaustive formal verification.

Final system simulation: Module verification, Full simulation from a simulation, Full Simulation from a formal verification.

IEEE 1850 PSL Property specifications and IEEE 1800 Verilog assertions: Introduction, Operations and keywords, PSL Boolean and temporal layer, Introduction to IEEE 1800 System Verilog, Sequence and property, BNF 185 and BNF 223.

Introduction to Verification Methodology: Open verification Methodology (OVM), Universal verification methodology (UVM)

Text Books:

1. Douglas L Perry Harry D Foster, Applied Formal Verification, McGraw Hill, 2005.
2. William K Lam, Hardware Design Verification: Simulation and Formal Method-based Approaches, Prentice Hall, 2008.
3. IEEE Standard for Universal Verification Methodology Language Reference Manual," in *IEEE Std 1800.2-2017* , vol., no., pp.1-472, 26 May 2017

EC 5264	Embedded Systems and RTOS	Elective - VI	3-0-0	3 Credits

Prerequisites: Nil

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify the functioning of embedded systems for different applications.
CO2	Develop embedded system programming skills.
CO3	Design, implement and test an embedded system.
CO4	Identify the unique characteristics of real-time embedded systems.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1						2	3	2	1			2
CO2						2	3	2	2			2
CO3						3	3	2	3			2
CO4						2	3	2	1			2

Detailed Syllabus:

Introduction to Embedded Computing: Embedded systems Overview, Characteristics ofembedded computing applications, Design Challenges, Common Design Metrics, Processor Technology, IC Technology, Trade-offs.

Process of Embedded System Development: The development process, Requirements, Specification, Architecture Design, Designing Hardware and Software components, system Integration and Testing.

Hardware platforms: Types of Hardware Platforms, Single board computers, PC Add-oncards, custom-built hardware platforms, ARM Processor, CPU performance, CPU power consumption, Bus-based computer systems, Memory devices, I/O devices ,component interfacing, Designing with microprocessors, system level performance analysis.

Program Design and Analysis: components for Embedded programs, Models ofprograms, Assembly, Linking, and loading, basic compilation techniques, software performance optimization ,program level energy and Power analysis, Program validation and Testing.

Real-Time Operating Systems: Architecture of the kernel, Tasks and Task Scheduler,Scheduling algorithms, Interrupt Service Routines, Semaphores, Mutex, Mailboxes, Message queues, Event Registers, Pipes, Signals, Timers, Memory management, Priority Inversion problem. Overview of off-the shelf operating systems-MicroC/OS II, Vxworks, RT Linux.

Overview of Hardware –Software co design

Text Books:

1. Wayne Wolf: Computers as Components-Principles of Embedded Computer System Design, Morgan Kaufmann Publisher-2006.
2. David E-Simon: An Embedded software Primer, Pearson Education, 2007.
3. K.V.K.K. Prasad Real-Time Systems: Concepts Design and Programming, Dreamtech Press, 2005.

EC 5265	RELIABILITY OF DEVICES AND CIRCUITS	Elective - VI	3-0-0	3 Credits

Prerequisites: Nil

Course Outcomes: At the end of the course the student will be able to:

CO1	Define the reliability of electronic device and circuit
CO2	Understand the failure mechanisms of electronic device and circuit
CO3	Understand the concept of yield in electronic manufacturing
CO4	Resolve the reliability is issues in VLSI design
CO5	Predict the circuit performance using reliability models

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1					1							
CO2					1			1				
CO3		1										
CO4					2			2				
CO5	2					2		2				

Detailed Syllabus:

Background and Introduction: Definitions of reliability, failure modes, mechanisms, Basic concepts – Reliability functions, Relationship between these functions – Baths tubs curve – Exponential failure density and distribution functions - Expected value and standard deviation of Exponential distribution – Measures of reliability – MTTF, MTTR, MTBF

Introduction to mathematical methods for reliability: Failure rates, Normal distribution function, Six Sigma, Exponential, Weibull and Lognormal distributions for reliability modeling. Manufacturing yields.

Physics of failure based models for : Mass transport-induced failures (electromiration and stress voiding), Electronic charge-induced failures (Dielectric breakdown, Hot carrier effects, Electrical over-stress and Electrostatic discharge), Environmental damage (moisture ingress, corrosion, radiation damage), Degradation of interconnects (solder creep and fatigue).

Circuit Performance considering NBTI, PBTI, oxide breakdown, random telegraph noise, radiation damage, impact of parasitic effects, process temperature variation, Electromagentic compatibility (EMC), Electromagnetic Interference (EMI) and Electrostatic Discharge (ESD).

Introduction to semiconductor device packaging: Materials and processes used for semiconductor device packaging, stresses induced because of packaging.

Text Books:

1. M. Ohring, Reliability and Failure of Electronic Materials and Devices, First Edition, Academic Press, 1998.
2. J.W. McPherson, Reliability Physics and Engineering, Second Edition, Springer, 2013.
3. Yuan Taur and T. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, 1998.
4. J.Ross, Microelectronic Failure Analysis, Sixth Edition, ASTM International, 2011.

EC5266	MODERN COMPUTER ARCHITECTURE	Elective - VI	3-0-0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Develop basic understanding of microprocessor architecture
CO2	Design Microprocessor and Microcontroller based systems
CO3	Understand the concept of memory management and interfacing in modern computers

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2			2	3			1				2
CO2	1			2	3	3		1				2
CO3	1	2		2	3	3						2

Detailed Syllabus:

Microcomputer Organization: CPU, Memory, I/O, Operating System, Multiprogramming, Multithreading, MS Windows

80386 Micro Processors : Review of 8086, salient features of 80386, Architecture and Signal Description of 80386, Register Organization of 80386, Addressing Modes

80386 Memory management, Protected mode, Segmentation, Paging, Virtual 8086 Mode, Enhanced Instruction set of 80386, the Co- Processor 80387

Pentium & Pentium-pro Microprocessor: Salient features of Pentium microprocessor, Pentium architecture, Special Pentium registers, Instruction Translation look aside buffer and branch Prediction, Rapid Execution module, Memory management, hyper-threading technology, Extended Instruction set in advanced Pentium Processors

Microcontrollers: Overview of microcontrollers - 8051 family microcontrollers, 80196 microcontrollers family architecture, instruction set, pin out, memory interfacing.

ARM Architectures

Text Books:

1. Barry B.Brey: Intel Microprocessor Architecture, Programming and Interfacing-8086/8088,80186,80286,80386 and 80486, PHI,1995.
2. Muhammad Ali Mazidi and Mazidi: The 8051 Microcontrollers and Embedded systems, PHI, 2008
3. Intel and ARM Data Books on Microprocessors and Microcontrollers.

EC5253	MIXED SIGNAL DESIGN LAB	Core	0-0-4	2 Credits

Prerequisites: Mixed signal Design

Course Outcomes: At the end of the course the student will be able to:

CO1	Implement discrete time signal processing circuits
CO2	Implement layout techniques specific to mixed signal IC design
CO3	Design OP-amp for mixed signal environment
CO4	Design a high speed comparator with high resolving capability
CO5	Design data converters and RF circuits for mixed signal environment.

Mapping of COs with POs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	3	1	1	2			2		2	1
CO2		1	3	1		3			2			1
CO3			2	1	1	1			2			1
CO4		1	2	1		1			2	2		1
CO5	1	1	3			2			2		2	1

Detailed Syllabus:

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   i. Two stage cross coupled clamped comparator
   ii. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   i. Parasitic sensitive integrator
   ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Bandgap reference circuit
5) Layouts of All the circuits Designed and Simulated

Text Books:

1) David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2) R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processsing, Wiley, 1986.
3) Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4) Alan Hastlings, The art of Analog Layout, Wiley, 2005.

EC5254	Physical Design Automation Lab	Core	0-0-4	2 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Apply the constraints posed by the VLSI fabrication technology to design automation tools using graph algorithms
CO2	Simulate partitioning algorithms viz., KL algorithm and simulated annealing algorithms.
CO3	Optimize floor planning using time driven floor planning algorithm and hierarchical tree based methods
CO4	Optimize routing using two terminal and multi terminal algorithms.

Mapping of COs with Pos

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		2					3			2		1
CO2	1	1			1	1	2	1	2		2	2
CO3		1			1	3	3	1	2			2
CO4	1	1	1	1		3	2	1	2	2		2

Detailed Syllabus:

Cycle 1:

1) Graph algorithms

1) Graph search algorithms
    1) Depth first search
    2) Breadth first search
2) Spanning tree algorithm
    1) kruskal's algorithm
3) Shortest path algorithm
    1) Dijkstra algorithm
    2) Floyd- Warshall algorithm
4) Steiner tree algorithm

2) Computational geometry algorithm

1) Line sweep method
2) Extended line sweep method

Cycle 2:

1) Partitioning algorithms

1) Group migration algorithms
    1) Kernighan –Lin algorithm
    2) Extensions of Kernighan-Lin algorithm
        1) Fiduccias –Mattheyses algorithm
        2) Goldberg and Burstein algorithm
2) Simulated annealing and evolution algorithms
    1) Simulated annealing algorithm

2) Simulated evolution algorithm
3) Metric allocation method

2) Floor planning algorithms

1) Constraint based methods
2) Integer programming based methods
3) Rectangular dualization based methods
4) Hierarchical tree based methods
5) Simulated evolution algorithms
6) Time driven Floorplanning algorithms

3) Routing algorithms

1) Two terminal algorithms
    1) Maze routing algorithms
        1) Lee's algorithm
        2) Soukup's algorithm
        3) Hadlock algorithm
    2) Line-Probe algorithm
    3) Shortest path based algorithm
2) Multi terminal algorithm
    1) Stenier tree based algorithm
        1) SMST algorithm
        2) Z-RST algorithm

Text Books:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic, 1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.