NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

SCHEME OF INSTRUCTION AND SYLLABI

M.Tech. – VLSI System Design

Effective from 2021-22

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

VISION

Towards a Global Knowledge Hub, striving continuously in pursuit of excellence in Education, Research, Entrepreneurship and Technological services to the society

MISSION

- Imparting total quality education to develop innovative, entrepreneurial and ethical future professionals fit for globally competitive environment.
- Allowing stake holders to share our reservoir of experience in education and knowledge for mutual enrichment in the field of technical education.
- Fostering product-oriented research for establishing a self-sustaining and wealth creating centre to serve the societal needs.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Create an Educational environment to prepare the students to meet the challenges of modern electronics and communication Industry through state of art technical knowledge and innovative approaches.

MISSION

- To create learning, Development and testing environment to meet ever challenging needs of the Electronic Industry.
- To create entrepreneurial environment and industry interaction for mutual benefit.
- To be a global partner in training human resources in the field of chip design, instrumentation and networking.
- To associate with international reputed institution for academic excellence and collaborative research.

Department of Electronics and Communication Engineering

Brief about the Department:

The Department of Electronics and Communication Engineering is one of the country's larger ECE Departments among all NITs in India and one of the largest departments of the National Institute of Technology, Warangal (NITW). The ECE Department at NITW has been an international reputation of excellence in teaching, research and service. With excellent laboratory facilities and dedicated faculty, the department of ECE offers broad range of programs that include undergraduate (B.Tech) and post graduate (M.Tech) in Embedded Systems & Intelligent Instrumentation, VLSI System design, Communication Systems and research (Ph.D) programs. Some of the recent sponsored project undertaken by the department includes Radar Emitter Identification using Neural Networks sponsored by DLRL, Hyderabad and Special Manpower Development in VLSI sponsored by MIT-Govt. of India.

List of Programs offered by the Department:

Program	Title of the Program
B.Tech.	Electronics and Communication Engineering (ECE)
M.Tech.	Electronic Instrumentation & Embedded Systems (EI & ES)
	VLSI System Design (VLSI)
	Advanced Communication Systems (ACS)
Ph.D.	Electronics and Communication Engineering (ECE)

Note: Refer to the following weblink for Rules and Regulations of M.Tech. program:
https://www.nitw.ac.in/main/MTechProgram/rulesandregulations/

NOTE: Refer to the following link for the guidelines to prepare dissertation report:
https://www.nitw.ac.in/main/PGForms/NITW/

M.Tech. – VLSI System Design

PROGRAM EDUCATIONAL OBJECTIVES

PEO	PROGRAM EDUCATIONAL OBJECTIVES (PEOs)
PEO1	Design and generate GDS files for digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, algorithms and develop testing methods.
PEO2	Model passive and active devices suiting advances in IC fabrication technology.
PEO3	Develop VLSI architectures optimized for constrained environments, RF systems and protocols.
PEO4	Communicate effectively and convey ideas using innovative engineering tools.
PEO5	Pursue lifelong learning as a means of enhancing knowledge base and skills necessary to contribute to the improvement of their profession and community.

Program Articulation Matrix

Mapping of Mission statements with program educational objectives

PEO / Mission Statements	PEO1	PEO2	PEO3	PEO4	PEO5
To create learning, development and testing environment to meet ever challenging needs of the Electronic industry.	3	3	3	2	2
To create entrepreneurial environment and industry interaction for mutual benefit.	2	2	2	3	3
To be a global partner in Training the human resource in the fields of Chip Design, Instrumentation and Networking.	2	3	2	2	3
To associate with internationally reputed Institutions for academic excellence and collaborative research.	2	2	2	2	3

1-Slightly; 2-Moderately; 3-Substantially

M.Tech – VLSI System Design

Program Outcomes (POs)

POs	Program Outcomes (POs)
PO1	Engage in critical thinking and pursue investigations/ research and development to solve practical problems.
PO2	Communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO3	Demonstrate higher level of professional skills to tackle multidisciplinary and complex problems related to VLSI System Design.
PO4	Model and offer solutions to issues related to device, IC design, testing and EDA tool development
PO5	Comprehend the state of the art VLSI technologies
PO6	Characterize and design analog, digital, RF and mixed signal subsystems meeting given constraints under deep sub micron environment

SCHEME OF INSTRUCTION

M.Tech. VLSI System Design – Course Structure

I - Year, I – Semester

S. No.	Course Code		L	T	P	Credits	Cat. Code
1	EC5201	Microchip Fabrication Techniques	3	0	0	3	PCC
2	EC5202	Device Modelling	3	0	0	3	PCC
3	EC5203	Digital IC Design	3	0	0	3	PCC
4	EC5204	Analog IC Design	3	0	0	3	PCC
5		Elective–I	3	0	0	3	PEC
6		Elective-II	3	0	0	3	PEC
7	EC5205	Analog IC Design Laboratory	0	0	4	2	PCC
8	EC5206	Digital IC Design Laboratory	0	0	4	2	PCC
9	EC5248	Seminar	0	0	2	1	SEM
		Total	**18**	**0**	**8**	**23**	

I - Year, II – Semester

S. No.	Course Code		L	T	P	Credits	Cat. Code
1	EC5251	Physical Design Automation	3	0	0	3	PCC
2	EC5252	Mixed Signal Design	3	0	0	3	PCC
3	EC5253	Low power VLSI Design	3	0	0	3	PCC
4		Elective – III	3	0	0	3	PEC
5		Elective – IV	3	0	0	3	PEC
6		Elective – V	3	0	0	3	PEC
7	EC5254	Mixed Signal Design Laboratory	0	0	4	2	PCC
8	EC5255	Physical Design Automation Laboratory	0	0	2	1	PCC
9	EC5256	FPGA Design Lab	0	0	2	1	PCC
10	EC5298	Seminar	0	0	2	1	SEM
		Total	**18**		**9**	**23**	

Note: PCC – Professional Core Courses
PEC – Professional Elective Courses

SCHEME OF INSTRUCTION

M.Tech. VLSI System Design – Course Structure

II - Year, I – Semester

S. No.	Course Code	Course Name	L	T	P	Credits	Cat. Code
1	EC6247	Comprehensive Viva				2	CVV
2	EC6249	Dissertation Part A				12	DW
		Total				**14**	

II - Year, II – Semester

S. No.	Course Code		L	T	P	Credits	Cat. Code
1	EC6299	Dissertation Part B				20	DW
		Total				**20**	

Credits in Each Semester					
Credits	**Sem-I**	**Sem-II**	**Sem-III**	**Sem-IV**	**Total**
CORE COURSES	12	9	00	00	**21**
Elective	06	9	00	00	**15**
Lab courses	04	04	00	00	**08**
Seminar	01	01	00	00	**02**
Comprehensive viva-voce	00	00	02	00	**02**
Project	00	00	12	20	**32**
Total	**23**	**23**	**14**	**20**	**80**

Program Elective Courses

Elective-1 (I Year, I Semester)		
S. No.	**Course Code**	**Course**
1	EC5211	FPGA Design
2	EC5212	Power Management IC Design
3	EC5213	Nano-electronic Materials and Devices
4	EC5214	Electronic Design Automation
Elective-2 (I Year, I Semester)		
S. No.	**Course Code**	**Course**
1	EC5215	VLSI Test & Testability
2	EC5216	VLSI Architectures
3	EC5217	Hardware Description Languages
4	EC5218	CAD for VLSI
Elective-3 (I Year, II Semester)		
S. No.	**Course Code**	**Course**
1	EC5261	Fundamentals of Nanoelectronics
2	EC5262	Full Custom Design
3	EC5263	ASIC System Design
4	EC5264	Electronic Systems Packaging
Elective-4 (I Year, II Semester)		
S. No.	**Course Code**	**Course**
1	EC5265	Hardware/Software Co-design
2	EC5266	CMOS RFIC Design
3	EC5267	VLSI Design Verification
4	EC5268	Advanced VLSI Interconnects
Elective-5 (I Year, II Semester)		
S. No.	**Course Code**	**Course**
1	EC5269	Embedded System and RTOS
2	EC5270	Reliability of Devices and Circuits
3	EC5271	Modern Computer Architecture
4	EC5272	Organic Electronics

DETAILED SYLLABUS

M.Tech. – VLSI System Design

Course Code: EC5201	Microchip Fabrication Techniques	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Explain the unit fabrication process steps
CO2	Explain the functions of packaging
CO3	Analyze process yield and yield measurement for a process
CO4	Propose the process flow for novel MOS devices
CO5	Construct the circuit layout using the design rules

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2		1		
CO2	1	1				
CO3	1	1		1		1
CO4						
CO5						

Syllabus:

Overview of semiconductor industry, unit process steps for fabrication

Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement; Contamination sources, Clean room construction; Oxidation: dry oxidation, wet oxidation; Photolithography: Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect.

Etching: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2; Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.

Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices.

Design rules, stick diagrams and layout.

Packaging: Chip characteristics, package functions, package operations

Learning Resources:

Text Books:

1. Microchip fabrication, Peter Van Zant McGraw Hill, 1997.
2. Silicon VLSI Technology: Fundamentals, Practice and Modeling , Plummer, J.D., Deal, M.D. and Griffin, P.B., Prentice-Hall , 2000, 3rd Ed.
3. ULSI technology , C.Y. Chang and S.M. Sze, McGraw Hill, 2000.
4. VLSI Fabrication principles, S.K. Gandhi, John Wiley and Sons, NY, 1994.
5. VLSI technology, S.M. Sze, McGraw-Hill Book company, NY, 1988.

Course Code: EC5202	Device Modeling	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Develop mathematical models for modern MOS devices.
CO2	Develop solution to overcome short channel issues.
CO3	Develop various compact models appropriate for industry.
CO4	Analyse current distribution in the devices like transistors, MOS devices.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	1	1	3
CO2	2	3	1	1	1	2
CO3	2	3	2	2	1	1
CO4	1	2	1	1	1	1

Syllabus:

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

The MOS transistor: Small signal modelling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

The bipolar transistor: Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics

Compact Modeling: Compact model Level 1, Level 2, Level 3, UTB/FD SOI MOSFET, FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

Learning Resources:

Text Books:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.

2. M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017.

3. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.

4. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

5. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

Course Code: EC5203	Digital IC Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Design CMOS inverters with specified noise margin and propagation delay.
CO2	Synthesize digital circuit using Verilog HDL.
CO3	Implement efficient techniques at circuit level for improving power and speed of
CO4	Design Synchronous Systems meeting timing constraints.
CO5	Design memories with efficient architectures to improve access times, power consumption.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	2	3	2	
CO2	2	1	1	1	2	2
CO3	2	1	1	2	3	1
CO4	1	1	2	2	2	1
CO5	1	1	1	2	3	

Syllabus:

MOS INVERTERS: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations, FinFET

DESIGNING COMBINATIONAL & SEQUENTIAL LOGIC GATES in CMOS: Static CMOS Design, Dynamic CMOS Design, Power Consumption in CMOS Gates

Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles, Nonbistable Sequential Circuits, Logic Style for Pipelined Structures.

TIMING ISSUES IN DIGITAL CIRCUITS: Introduction, Synchronous Timing basics, Clock Skew and Jitter, Clock distribution techniques, Clock Generation and Synchronization.

DESIGNING ARITHMETIC BUILDING BLOCKS: Introduction, The Adder: Circuit and Logic Design, Multipliers: Shifters, Power Considerations in Datapath Structures.

DESIGNING MEMORY: Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM, Memory Peripheral Circuitry.

Advanced Digital IC Design: Block level design

Learning Resources:

Text Books:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.

2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

Course Code: EC5204	Analog IC Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different
CO2	Design all basic building blocks like sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and should be able to design OpAmp fully
CO4	Identify the suitable different topologies of the constituent sub systems and corresponding
CO5	Design Analog integrated system completely upto tape-out including parasitic effects.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3		2	1
CO2	2	1	3		2	2
CO3	2	1	3		2	1
CO4	1	1	3		3	2
CO5	1	1	3		2	1

Syllabus:

MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices.

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references.

Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, Cascode, folded cascode, choice of device models.

Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, replication principle, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion, gilbert cell

Operational amplifier-characterization, 2 stage OP amp, process and temperature independent compensation, output stage.

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, constant g_m biasing, speed and noise issues, case study, curvature correction.

PTAT, CTAT, Bandgap circuit, start-up circuit, curvature correction Design. Negative feedback amplifier design with Nyquist criteria analysis.

Learning Resources:

Text Books:

1. Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.
4. Design of Analog CMOS Integrated Circuit, Behad Razavi McGraw Hill Education, 2nd Edition 2017

Course Code: EC5205	Analog IC Design Lab	Credits 0-0-4: 2

Prerequisites: EC5204 Analog IC Design

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different
CO2	Design all basic building blocks viz., sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and design OPamp fully compensated
CO4	Specify suitable topologies of the constituent sub systems and corresponding circuits as per
CO5	Design Analog integrated circuits taking account the parasitic effects.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3		2	2
CO2	2		2		2	2
CO3	1	1	2		2	2
CO4	1		2		3	1
CO5	1	1	3		2	3

Syllabus: **All circuits till post layout**

Cycle 1:

Lambda calculation for PMOS & NMOS, F_T calculation, Transconductance plots, Single transistor amplifier, Ideal current source, PMOS current source, NMOS saturated load, Degenerative resistor, Cascade amplifier: Ideal current source, PMOS current source.

Cycle 2:

Current sinks: Basic current sink, Current sink with negative feedback, Bootstrap current sink, Cascode current sink, Regulated cascode current sink.

Current sources: Basic current source, Current source with negative feedback, Bootstrap current source, Cascade current source, Regulated cascade current source,

Current mirrors: Basic current mirror, Wilson current mirror, Cascode current mirror, Regulated cascade current mirror, Widlar current source

Feedback topologies

Differential amplifier, Two stage Operational amplifier design

Learning Resources:

Text Books:

1. Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

Course Code: EC5206	Digital IC Design Lab	Credits 0-0-4: 2

Prerequisites: EC5203 Digital IC Design

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Design of combinational and sequential circuits using Verilog HDL/ VHDL
CO2	Synthesize digital circuit targeting state of the art FPGA
CO3	Design combinational and sequential circuits at circuit level using EDA tools
CO4	Implement efficient techniques at circuit level for improving power and speed of

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1		1	2	1
CO2	2	1		2	1	1
CO3						
CO4	2			2	3	2

Syllabus:

Cyle 1

Design and Simulation of CMOS Inverter to study the transfer Characteristics by varying the design constraints using EDA Tools

Design and Simulation of logic gates using various logic styles and compare the performance

Design a Full Adder cell using various configurations proposed in the literature and simulate to compare the performance using EDA tools

Cycle 2:

Design, Develop HDL model, Simulate and Synthesize

32-bit Parallel adder using 8-bit adder module, 32-bit Shift register using 8-bit Shift register module

RTL to GDS-II: Design any System as a case Study

EDA Tools: Mentor Graphics Tools

Learning Resources:

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003.

2. Douglas Perry, VHDL: Programming by Example, 2017

Course Code: EC5211	FPGA Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand FPGA design flow.
CO2	Identify the building blocks of commercially available FPGA/CPLDs.
CO3	Develop VHDL/Verilog models and synthesize targeting for Vertex, Spartan FPGAs.
CO4	Develop parameterized library cells and implement system designs using parameterized

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	2	1	1	
CO2	2	1	2	3	3	
CO3	2	1	2	3	2	1
CO4	3		1	2	2	

Syllabus:

INTRODUCTION TO FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.

DEISGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter.

FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA

CASE STUDY – Applications using Kintex-7, Viretex-7, Artix-7.

Learning Resources:

Text Books:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.

2. Data sheets of Artix-7, Kintex-7, Virtex-7 .

3. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

Course Code: EC5212	Power Management IC Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand why power management circuits are needed in a VLSI system
CO2	Understand different components of a power management system with focus on dc-dc converters
CO3	Design a chip level dc-dc converter from a given system level specifications
CO4	Apply top-down design approach of a dc-dc converter topology

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	1	1	1	
CO2		1	1	2	3	1
CO3	1	1	2		1	
CO4						

Syllabus:

Unit-1: Introduction to Power Management and Voltage Regulators Need of power management, power management applications, classification of power management, power delivery of a VLSI system, power conversion, discrete vs. integrated power management, types of voltage regulators (switching Vs linear regulators) and applications, converter's performance parameters (voltage accuracy, power conversion efficiency, load regulation, line regulation, line and load transient response, settling time, voltage tracking), local Vs remote feedback, kelvin sensing, Point-of-Load (POL) regulators.

Unit-2: Linear Regulators Low Drop-Out Regulator (LDO), Source and sink regulators, shunt regulator, pass transistor, error amplifier, small signal and stability analysis, compensation techniques, current limiting, power supply rejection ratio (PSRR), NMOS vs. PMOS regulator, current regulator.

Unit-3: Switching DC-DC Converters and Control Techniques Types (Buck, boost, buck-boost), power FETs, choosing L and C, PWM modulation, leading, trailing and dual edge modulation, Losses in switching converters, output ripple, voltage Vs current mode control, CCM and DCM modes, small signal model of dc-dc converter, loop gain analysis of un-compensated dc-dc converter, type-I, type-II and type-III compensation, compensation of a voltage mode dc-dc converter, compensation of a current mode dc-dc converter, hysteretic control, switched capacitor dc-dc converters.

Unit-4: Top-down Design Approach of a DC-DC Converter Selecting topology, selecting switching frequency and external components, sizing power FETs, segmented power FET, designing gate driver, PWM modulator, error amplifier, oscillator, ramp generator, feedback resistors, current sensing, PFM/PSM mode for light load, effect of parasitic on reliability and performance, current limit and short circuit protection, soft start control, chip level layout and placement guidelines, board level layout guidelines, EMI considerations.

Unit-5: Introduction to Advanced Topics in Power Management Digitally controlled dc-dc converters, digitally controlled LDOs, adaptive compensation, dynamic voltage scaling (DVS), Single-Inductor Multiple-Outputs (SIMO) Converters, dc-dc converters for LED lighting, Li-ion battery charging circuits.

Learning Resources:

Text Books:

1. Switch-Mode Power Supplies: SPICE Simulations and Practical Designs, Christophe P Basso, BPB Publications, 2010

2. Power Management Techniques for Integrated Circuit Design By Ke-Horng Chen, Wiley-Blackwell, 2016

3. Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer (India) Pvt. Ltd, 2005

Course Code: EC5213	Nano-electronic Materials and Devices	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the physics and materials for Nanoelectronics
CO2	Understand the scaling issues
CO3	Explain the need for non-classical and non-silicon based devices
CO4	Analyse the performance of novel devices

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			1			
CO2						1
CO3	1	1				
CO4						

Syllabus:

Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore's Law and Koomey's law.

Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Metal gate transistor : Motivation, requirements, Integration Issues.

Non classical MOS transistor: Requirements, and Novel devices

SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues.

Vertical transistors - FinFET and Cylindrical gate FET.

Novel devices: Tunnel FET, Negative-Capacitance (NC) FET.

Metal source/drain junctions - Properties of schotky junctions on Silicon, Germanium and

compound semiconductors -Workfunction pinning.

Germanium Nano MOSFETs : strain , quantization , Advantages of Germanium over Silicon, PMOS versus NMOS.

Compound semiconductors - Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs, exploiting novel materials, strain, quantization.

Emerging nano materials : CNT, Graphene, Nanotubes, nanorods and other nano-structures.

Learning Resources:

Text Books:

1. Y. Taur and T. Ning, "Fundamentals of Modern VLSI devices" Cambridge University Press

2. Nicollian and J. R. Brews "MOS (Metal Oxide Semiconductor) Physics and Technology" Wiley Publishers

3. Brundle, C.Richard; Evans, Charles A. Jr.; Wilson, Shaun “Encyclopedia of Materials Characterization”, Elsevier.

4. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017.

5. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009

6. Related research papers.

Course Code: EC5214	Electronic Design Automation	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	To learn a number of circuit analysis techniques such as nodal analysis, mesh analysis,
CO2	To formulate equations and solve nonlinear networks.
CO3	To determine the convergence and stability boundary for multi-step or multi-stage methods
CO4	To introduce special classes of multistep methods for the solution of electrical networks.
CO5	To introduce general purpose circuit simulators and learn the fundamental equations for

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3		1	
CO2	2		2		1	1
CO3	1		3		2	1
CO4			1		1	
CO5	1		2		3	

Syllabus:

Formulation of network equations: Nodal, mesh, modified nodal and hybrid analysis equations; Sparse matrix techniques; Solution of nonlinear networks through Newton-Raphson technique; Multistep methods: convergence and stability; Special classes of multistep methods: Adams-bashforth, Adams-Moulton and Gear's methods; Solution of stiff systems of equations; Adaptation of multistep methods to the solution of electrical networks; General purpose circuit simulators.

Review of semiconductor equations (Poisson, continuity, drift-diffusion, trap rate). Finite difference formulation of these equations in 1D and 2D. Grid generation; Physical/empirical models of semiconductor parameters (mobility, lifetime, band gap, etc.); Computation of characteristics of simple devices (p-n junction, MOS capacitor, MOSFET, etc.); Small-signal analysis.

Learning Resources:

Text Books:

1. L.O. Chua and P.M. Lin, Computer aided analysis and electronic circuits, Prentice Hall, 1975.

2. S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer-Verlag, 1984.

3. N.J. McCalla, Fundamentals of Computer Aided Circuit Simulation, Kluwer Academic Publishers, 1988.

Course Code: EC5215	VLSI Test and Testability	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same.
CO3	Specify fabrication defects, errors and faults
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	2	2	1	
CO2	1	3	1	2	2	
CO3	2	2	1	2	2	
CO4	1	1	1	1	2	2
CO5	1	1	1	2	2	2

Syllabus:

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.

Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.

Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method.

D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches Test pattern generation for BIST, Circular BIST. BIST Architectures. Testable memory design-Test algorithms-Test generation for Embedded RAMs. .

Learning Resources:

Text Books:

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.

Reference Books:

1. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002
2. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000.
3. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

Course Code: EC5216	VLSI Architectures	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Design of RISC architecture and controller for a specific instruction set.
CO2	Improve the performance of RISC processor by employing pipelining.
CO3	Translate DSP algorithm into an efficient architecture and study the design of
CO4	Estimate the effect of folding, unfolding and retiming techniques on the performance of DSP architectures.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	1	1	2	1
CO2	2	2	1	3	3	1
CO3	2	1		2	2	
CO4	3	1		2	2	

Syllabus:

Overview of the features of Instruction set architectures of CISC, RISC and DSP processors

CPU performance and its factors, evaluating the performance.

Design of RISC processor**:** Building datapath and Control, multicycle implementation

Enhancing the performance with pipelining**:** An overview of pipelining, pipelined datapath, Pipelined Control unit, various hazards of pipelining, Hazard free pipelined RISC implementation

Multiprocessors: Introduction, Multiprocessors connected by a single bus, Multiprocessors connected by a network, Network Topologies, Evolution versus revolution in Computer Architecture

Representation of DSP Algorithms, data flow graph representations, loop bound and iterative bound, algorithms for computing iteration bound

Pipe lining and parallel processing: Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power

Different techniques to improve the performance VLSI Architectures: Retiming, Unfolding and Folding techniques

Learning Resources:

Text Books:

1. D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier, 2011.
2. Keshab Parhi, VLSI digital signal processing systems design and implementations, Wiley 1999

Course Code: EC5217	Hardware Description Languages	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Differentiate sequential language and concurrent language.
CO2	Design combinational logic circuits using VHDL.
CO3	Design sequential logic circuits using VHDL.
CO4	Model Analog circuits using Verilog AMS.
CO5	Differentiate sequential language and concurrent language.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1		2	2	1	2	
CO2	1	1	1	1	3	
CO3	1	1	1	1	2	
CO4	2	2	2	1	1	
CO5						

Syllabus:

Verilog: About Verilog, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading.

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits.

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot.

System Verilog: Verilog +, Coverage, Randomization, Assertion, functional coverage, Object oriented programming, define – parameter.

Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling.

Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior.

Learning Resources:

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003.

2. Chris Spear, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd ed., Springer, 2012

3. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004.

Course Code: EC5218	CAD for VLSI	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Specify layout techniques in IC.
CO2	Identify algorithms required for circuit simulators.
CO3	Incorporate timing analysis and floor planning.
CO4	Apply scripting language PERL to improve EDA tool flow.
CO5	Specify layout techniques in IC.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2					2
CO2	1	1				2
CO3	1					3
CO4	1	1				2
CO5						

Syllabus:

Introduction to Design Methodologies: The VLSI Design Problem, Design Methods and Technologies, Layout Methodologies, Top-Down Approach: Routing: Fundamentals, Global Routing, Detailed Routing.

Performance Issues in Circuit Layout: Delay Models, Timing Driven Placement, Timing Driven Routing, Power Minimization.

Single-Layer Routing and Applications: Planar Subset Problem, Single-Layer Global Routing, Over-the-cell Routing, Multichip Modules, Wire-Length and Bend Minimization Techniques.

Cell Generation and Programmable Structures: Programmable Logic Arrays, Transistor Chaining, Weinberger Arrays and Gate Matrix Layout, CMOS Cell Layout Styles Considering Performance Issues, Compaction: 1D Compaction, 2D Compaction.

Learning Resources:

Text Books:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2006.

2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.

Course Code: EC5251	Physical Design Automation	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Students should have understood the relationship between design automation algorithms and
CO2	Should be able to adapt the design algorithms to meet the critical design parameters.
CO3	Should have learnt various layout optimization techniques and should be able to map them
CO4	Should be in a position to develop proto-type EDA tool and test its efficacy.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			1	1	3
CO2	2			1		2
CO3	1			1		3
CO4	1				1	2

Syllabus:

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules.

Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Learning Resources:

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

Course Code: EC5252	Mixed Signal Design	Credits 3-0-0: 3

Prerequisites: Analog and Digital IC Design

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the necessity of mixed signal systems and demonstrate corresponding layout
CO2	Design basic cells like OpAmp to meet the mixed signal specifications.
CO3	Design comparators to meet the high speed requirements of digital circuitry.
CO4	Design a complete mixed signal system that includes efficient data conversion and RF

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1		1	
CO2	1	1	3		1	
CO3	1	1	3		3	
CO4	1		3		2	

Syllabus:

Review: Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower, Source-Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage

Process and temperature independent compensation, Ahuza's compensation, nested miller compensation, dynamic offset cancellation techniques.

Basic Building Blocks, OpAmp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator , Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit.

Performance of Sample-and-Hold Circuits, Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and BiCMOS Sample-and-Holds, Translinear Gain Cell, Translinear Multiplier

Comparator Specifications Input Offset and Noise , Hysteresis, ,Using an OpAmp for a Comparator, Input-Offset Voltage Errors, Charge-Injection Errors, Making Charge-Injection Signal Independent , Minimizing Errors Due to Charge-Injection, speed of Multi-Stage Comparators, Latched Comparators, Latch-Mode Time Constant, Latch Offset, Examples of CMOS and BiCMOS Comparators, Input-Transistor Charge Trapping, Examples of Bipolar Comparators,

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity

Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters.

Multi-Bit Successive-Approximatio**n,** Algorithmic (or Cyclic) A/D Converter, Ratio-Independent Algorithmic Converter, Pipelined A/D Converters, One-Bit-Per-Stage Pipelined Converter,1.5 Bit Per Stage Pipelined Converter, Pipelined Converter Circuits,

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL characterization and Design Example. Jitter and Phase Noise, Period Jitter , P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter,

Probability Density Function of Jitter, Ring Oscillators , LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLS

Learning Resources:

Text Books:

1. Design of CMOS Phase-Locked Loops From Circuit level to Architecture Level, Behzad Razavi, Cambridge University Press, 2020.
2. Understanding Delta-Sigma Data Converters, Richard Schreier, Shanthi Pavan and Gabor C Temes, Wiley, 2nd Edition, 2017.
3. David A Johns, Ken Martin: Analog IC design, Wiley 2008.
4. R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986
5. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008

Course Code: EC5253	Low power VLSI Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Identify clearly the sources of power consumption in a given VLSI Circuit.
CO2	Analyze and estimate dynamic and leakage power components in a DSM VLSI Circuit.
CO3	Choose the types of SRAMs/ DRAMs for the given Low power applications.
CO4	Design low power arithmetic circuits and systems.
CO5	Decide at which level of abstraction is advantageous to implement low power

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1		1	1	
CO2	1	1		1	2	
CO3		2		2	3	
CO4				3		
CO5				1		

Syllabus:

Low Power CMOS VLSI design: Introduction: Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation.

Circuit Techniques for Low Power Design: Design for Low Power, Multiple Vth techniques, Dynamic Vth techniques

Standard Adder Cells, Review of CMOS Adders Architectures and performance Comparison, Low Voltage Low Power Design Techniques, Current Mode Adders.

Review of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison.

Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques

Architectural Techniques for Low Power: Parameters effecting power dissipation, Variable frequency, Dynamic voltage Scaling, Dynamic Voltage and Frequency Scaling, Reduced VDD, Architectural clock gating, Power gating, Multi-voltage, Optimizing memory power.

Low Power Implementation Techniques: Library Selection, Clock Gating, Timing Impact due to Clock gating, Gate-level power optimization techniques, Power Optimization for Sleep Mode

Learning Resources:

Text Books:

1. Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Edition 2009, Tata Mc Graw Hill
2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002

Reference Books:

1. Jan Rabaey, Low Power Design Essentials, Springer.

Course Code: EC5254	Mixed Signal Design Laboratory	Credits 0-0-4: 2

Prerequisites: Mixed signal Design

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Implement discrete time signal processing circuits
CO2	Implement layout techniques specific to mixed signal IC design
CO3	Design OP-amp for mixed signal environment
CO4	Design a high speed comparator with high resolving capability
CO5	Design data converters and RF circuits for mixed signal environment.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	3	1	1	2
CO2		1	3	1		3
CO3			2	1	1	1
CO4		1	2	1		1
CO5	1	1	3			2

Syllabus:

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   i. Two stage cross coupled clamped comparator
   ii. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   i. Parasitic sensitive integrator
   ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Bandgap reference circuit
5) Layouts of All the circuits Designed and Simulated

Learning Resources:

Text Books:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processsing, Wiley, 1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

Course Code: EC5254	Physical Design Automation Lab	Credits 0-0-2: 1

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Apply the constraints posed by the VLSI fabrication technology to design automation tools
CO2	Simulate partitioning algorithms viz., KL algorithm and simulated annealing algorithms.
CO3	Optimize floor planning using time driven floor planning algorithm and hierarchical tree
CO4	Optimize routing using two terminal and multi terminal algorithms.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1		2				
CO2	1	1			1	1
CO3		1			1	3
CO4	1	1	1	1		3

Syllabus:

Cycle 1:

1) Graph algorithms

1) Graph search algorithms
    1) Depth first search
    2) Breadth first search
2) Spanning tree algorithm
    1) kruskal's algorithm
3) Shortest path algorithm
    1) Dijkstra algorithm
    2) Floyd- Warshall algorithm
4) Steiner tree algorithm

2) Computational geometry algorithm

1) Line sweep method
2) Extended line sweep method

Cycle 2:

1) Partitioning algorithms

1) Group migration algorithms
    1) Kernighan –Lin algorithm
    2) Extensions of Kernighan-Lin algorithm
        1) Fiduccias –Mattheyses algorithm
        2) Goldberg and Burstein algorithm
2) Simulated annealing and evolution algorithms
    1) Simulated annealing algorithm
    2) Simulated evolution algorithm
3) Metric allocation method

2) Floor planning algorithms

1) Constraint based methods
2) Integer programming based methods
3) Rectangular dualization based methods
4) Hierarchical tree based methods

5) Simulated evolution algorithms
6) Time driven Floorplanning algorithms

3) Routing algorithms

1) Two terminal algorithms
    1) Maze routing algorithms
        1) Lee's algorithm
        2) Soukup's algorithm
        3) Hadlock algorithm
    2) Line-Probe algorithm
    3) Shortest path based algorithm
2) Multi terminal algorithm
    1) Stenier tree based algorithm
        1) SMST algorithm
        2) Z-RST algorithm

Learning Resources:

Text Books:

1. Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic, 1998.
2. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

Course Code: EC5256	FPGA Design Lab	Credits 0-0-2: 1

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Students get exposure to the resources of latest FPGA devices and FPGA Design Flow
CO2	Development of RTL model and generation of RTL Schematic
CO3	Applying design constrains to meet the target performance
CO4	Post Synthesis timing analysis and Post Layout timing analysis
CO5	Applying various low power techniques and analyse the performance

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3				2
CO2			2	2		2
CO3	2	2	2	2	3	3
CO4				1	2	3
CO5	2			3	3	3

Syllabus:

Cycle 1

Design, Simulate, Synthesize the following Combinational Ckts targeting 7 series FPGA

8-bit -bit low power high speed adder

High Speed and low power 16/32/64-bit adder using an 8-bit adder

16x16 bit multiplier using IP Core, CORDIC multiplier

Design, Simulate, Synthesize the following Sequential circuits targeting 7 series FPGA

a clock divider, FIFO using IP core

Cycle 2

Implement any System targeting Artix-7 series FPGA employing low power techniques while meeting target speed

Learning Resources:

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003.

2. Douglas Perry, VHDL: Programming by Example, 20173.

3. www.xilinx.com

Course Code: EC5261	Fundamentals of Nanoelectronics	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the concept of electrical and thermal conductivity in metal
CO2	Understand the crystal structure and bravais lattice types
CO3	Study the concept of energy band gaps and Tight Binding Model
CO4	Analyse the Ferromagnetism in solids

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			1			
CO2						1
CO3	1	1				
CO4			2			1

Syllabus:

Drude's model: Introduction to Drude's theory of electrons in a metal, Postulates of Drude's theory, Calculating electrical conductivity of metal using Drude's Model, Hall effect in metals, Understanding thermal conductivity of a metal using Drude's model

Sommerfeld's model: Fermi energy and Fermi Sphere, Density of states; Specific heat of an electron gas and the behaviour of thermal conductivity of a solid and relationship with electrical conductivity; Introduction to magnetism in metal

Crystal structure and their classifications: Understanding crystal structure using Bravais Lattice, Bravais lattice types, different crystal types, indexing crystal planes

Vibrations of crystals with monoatomic basis, Acoustic and optical modes; Two atoms ates, per primitive basis, Quantization of Elastic waves, Density of states of phonons, Phonon Momentum

Bloch's theorem for wavefunction of a particle in a periodic potential, Nearly free electron model, origin of energy band gaps; Kronig-penney Model, Tight Binding Model

Magnetism in materials; Superconductivity.

Learning Resources:

Text Books:

1. John Singleton, Band Theory and Electronic Properties of Solids, Oxford, 2001.

2. Prasanta K. Misra, Physics of Condensed Matter, Elsevier, 2012.

3. M. L. Cohen and S. G. Louie, Fundamentals of Condensed Matter Physics, Cambridge university Press, 2016.

4. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017.

Course Code: EC5262	Full Custom Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand efficient Layout design techniques.
CO2	Absorb the process variations into the layout.
CO3	Construct guard rings, pad rings suiting mixed signal environment.
CO4	Design layouts minimizing stress effects.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	1	3
CO2		1		1		2
CO3	1		2	1	1	3
CO4		1	1	1		3

Syllabus:

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

Advanced techniques for specialized building blocks: Standard cell libraries, Pad cells and Laser fuse cells, advanced techniques for building blocks, Power grid Clock signals and Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

Layout considerations due to process constraints: Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings , Constructing the pad ring , Minimizing Stress effects.

Proper layout: CAD tools for layout, planning tools, Layout generation tools, Support tools**.** Analog layout concepts.

Learning Resources:

Text Books:

1. Dan Clein, CMOS IC Layout Concepts Methodologies and Tools, Newnes, 2000.
2. Ray Alan Hastings, The Art of Analog Layout, 2nd Edition, Prentice Hall, 2006

Course Code: EC5263	ASIC System Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Architect ASIC library design.
CO2	Develop programmable ASIC logic cells.
CO3	Design I/O cells and interconnects.
CO4	Identification of new developments in SOC and low power design.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1		2			3	1
CO2				2	1	1
CO3	1	1			1	2
CO4		2		3	1	1

Syllabus:

Introduction : Types of ASIC's, Design Flow , CMOS Logic.

Traditional Design Flow : Specification and RTL Coding, Dynamic Simulation, Constraints, Synthesis and Scan Insertion, Formal Verification, Static Timing Analysis, Placement, Routing and Verification, Engineering Change Order, Physical Compiler Flow Physical Synthesis

Example Design: Initial Setup, Traditional Flow, Pre-Layout Steps, Post-Layout Steps Physical Compiler Flow

Technology Library: Technology Libraries, Logic Library Basics, Delay calculation

Partitioning and Coding Styles: Partitioning for Synthesis, General guidelines, Logic Inference

Constraining Designs: Environment and Constraints, Advanced Constraints, Clocking issues

OPTIMIZING DESIGNS: Design Space Exploration, Total Negative Slack, Compilation Strategies, Optimization techniques

Design for Test: Types of DFT, Scan Insertion

Programmable ASIC Design: CLB, IOB, Programmable Interconnect of Xilinx Devices

Learning Resources:

Text Books:

1. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, 2nd Edition, Kluwer Academic, 2002.
2. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.

Course Code: EC5264	Electronic Systems Packaging	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the role of packaging in the computer, telecommunication, automotive, medical and consumer electronics industry
CO2	Learn the fundamentals of electrical packaging design, design for reliability, thermal management
CO3	Analyze the performance of various TSVs for 3-D ICs
CO4	Identify the packaging materials with their appropriate properties

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3		1	
CO2	2		2		1	1
CO3	1		3		2	1
CO4	1		2		3	

Syllabus:

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology. Materials for Microelectronic packaging, Packaging materials properties, ceramics, polymers and metals in packaging. Electrical Anatomy of systems packaging, signal distribution, power distribution, electromagnetic interference.

3-D technology and Packaging Techniques: Silicon interposer technology, Through Silicon Vias (TSVs). Hybrid packaging technique, Silicon-Less Interconnect technology. 3D Integrated Architectures

Through Silicon Via: Materials, Properties and Fabrication: CNT, GNR, properties of TSVs, fabrication of TSVs, challenges for TSV implementation. Modeling and performance analysis of Copper-based, CNT-based, GNR-based TSVs. Liners in TSVs

Physical Design and Thermal Management Techniques for 3-D ICs
Case study: clock distribution networks for 3-D ICs, Trends in Packaging.

Learning Resources:

Text Books:

1. Three-Dimensional Integrated Circuit Design, Vasilis F Pavlidis, E G Friedman, Morgan Kaufmann Publishers, Elsevier, 2009.
2. Fundamentals of Microsystem Packaging, Rao R. Tummala, McGraw Hill, 2001.
3. Through-Slicon Vias for 3D Integration, John H. Lau, McGraw Hill, 2012.
4. Related research papers.

Course Code: EC5265	Hardware / Software Co-Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand Serial and parallel communication protocols.
CO2	Model data flow and implement the same through software and hardware.
CO3	Operate data flow using USB and CAN bus for PIC microcontrollers.
CO4	Design embedded Ethernet for Rabbit processors.
CO5	Design CORDIC and Crypto coprocessor.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			1			
CO2						1
CO3	1	1				
CO4			2			1
CO5		1				

Syllabus:

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design.

Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph4.4 Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph.

Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor.

System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

Learning Resources:

Text Books:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.

2. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

Course Code: EC5266	CMOS RFIC Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the design bottlenecks specific to RF IC design
CO2	Identify noise sources and develop noise models for the devices and systems.
CO3	Identify various Transmitter and receiver architectures
CO4	Design various RF amplifiers

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3		1	
CO2	2		2		1	1
CO3	1		3		2	1
CO4	1		2		3	

Syllabus:

Basic concepts of RF IC design: Design Bottle necks of RF IC design Non linearity and Time invariance Sensitivity and dynamic range, Passive impedance transformation, RF radio receiver front end non idealities and design parameters: Effects of nonlinearity, 1 dB compression point, Derivation of required noise figure at receiver front end, Required IIP_3 at receiver front end, Partitioning of required NF at receiver front end and IIP_3 into individual NF and IIP_3.

Noise: Noise sources in MOSFETs, Modeling of thermal noise and flicker noise, noise analog integrated circuits.

Transceiver architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests.

Low Noise Amplifier: Introduction, General Philosophy, Matching Networks, Comparison of Narrowband and wideband LNA.
Wideband LNA Design: DC Bias, Gain ad Frequency Response, Noise Figure.
Narrowband LNA: Principles, core amplifier design, noise figure, power dissipation, trade-offs between noise figure and power dissipation, noise contribution from other sources.

Mixers: Active mixer, modeling mixers, unbalanced mixer circuits, single balanced mixer circuit, double balanced mixer circuits, Quantitative description of Gilbert mixer, conversion gain, Distortion, analysis of Gilbert mixer. Passive mixers: switching mixer, distortion in unbalanced switching mixer, conversion gain and noise.
Frequency synthesizer: PLL based frequency synthesizer: Concepts of PLL, phase detector, charge pump, RF Synthesizer architectures, Frequency Dividers, VCO, LC oscillators, Ring oscillator, Phase noise, Loop filter and system design.

Learning Resources:

Text Books:

1. VLSI for wireless communication , Bosco Leung, PrenticeHall
2. RF Microelectronics by Behad Razavi , PrenticeHall

Course Code: EC5267	VLSI Design Verification	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Specify the formal verification techniques.
CO2	Implement formal test plan process.
CO3	Implement simulation based verification.
CO4	Model hardware interfaces with concurrency constructs.
CO5	Apply IEEE 1850 property specification language and IEEE1800 Verilog assertions.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2			1		3
CO2	1			1		2
CO3	3		1			3
CO4	1					3
CO5		1		1		

Syllabus:

Verification process: Verification plan, Debug Cycle, Simulation and Output data, Testbench development.

Current verification techniques: HDL Software simulator, Accelerated simulation, Process-Based Accelerator techniques, Hardware emulation, FPGA prototyping.

Introduction to formal techniques and property specification: Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process.

Techniques for proving properties: Abstraction reduction, Compositional reasoning, Counter abstraction, Gradual Exhaustive formal verification.

Final system simulation: Module verification, Full simulation from a simulation, Full Simulation from a formal verification.

IEEE 1850 PSL Property specifications and IEEE 1800 Verilog assertions: Introduction, Operations and keywords, PSL Boolean and temporal layer, Introduction to IEEE 1800 System Verilog, Sequence and property, BNF 185 and BNF 223.

Introduction to Verification Methodology: Open verification Methodology (OVM), Universal verification methodology (UVM)

Learning Resources:

Text Books:

1. Douglas L Perry Harry D Foster, Applied Formal Verification, McGraw Hill, 2005.
2. William K Lam, Hardware Design Verification: Simulation and Formal Method-based Approaches, Prentice Hall, 2008.
3. IEEE Standard for Universal Verification Methodology Language Reference Manual," in *IEEE Std 1800.2-2017* , vol., no., pp.1-472, 26 May 2017

Course Code: EC5268	Advanced VLSI Interconnects	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Get an insight on transmission line parameters of VLSI interconnects
CO2	Understand the novel solutions on future VLSI Interconnects
CO3	analyze the importance of Graphene and CNT for Interconnect applications
CO4	analyze the performance of various VLSI interconnects

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	1	3
CO2		1		1		2
CO3	1		2	1	1	3
CO4						

Syllabus:

Preliminary concepts: Interconnects for VLSI applications, metallic interconnects, optical interconnects, superconducting interconnects, advantages of copper interconnects, challenges posed by copper interconnects, fabrication process, even and odd mode capacitances, miller theorem, transmission line equations, resistive interconnection as ladder network, propagation modes in microstrip interconnection, slow wave mode propagation, propagation delays.
Parasitic extraction: Parasitic resistance, effect of surface/interface scattering and diffusion barrier on resistance, Capacitance: parallel-plate capacitance, fringing capacitance, coupling capacitance, methods of capacitance extraction, Inductance: self inductance, mutual inductance, methods of inductance extraction, high frequency losses, frequency dependent parasitics, skin effect, dispersion effect.
Modeling of interconnects and Crosstalk analysis: Elmore model, Transfer function model, even and odd mode model, Time domain analysis of multiconductor lines, Finite Difference Time Domain (FDTD) method, performance analysis using linear driver (Resistive) and nonlinear driver (CMOS), advanced interconnect techniques to avoid crosstalk.
Future VLSI Interconnects: Optical interconnects, Superconducting interconnects, Nanotechnology interconnects, Silicon nanowires, Carbon nanotubes, Graphene nanoribbons: system issues and challenges, material processing issues and challenges, design issues and challenges.
Carbon nanotube and Graphene nanoribbon VLSI interconnects: Quantum electrical properties: quantum conductance, quantum capacitance, kinetic inductance, Carbon nanotube (CNT) and Graphene nanoribbon (GNR) interconnects, electron scattering and lattice vibrations, electron mean free path, single-wall CNT and single layer GNR resistance model, multi-wall CNT and multi-layer GNR resistance model, transmission line interconnect models,
performance comparison of CNTs, GNRs and copper interconnects.

Learning Resources:

Text Books:

1. High-Speed VLSI Interconnects, Ashok K. Goel, 2007.
2. Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, Y.S. Diamand, 2009.
3. Carbon nanotube and Graphene Device Physics, H.S Philip Wong and Deji Akinwande, 2011.
4. Related research papers.

Course Code: EC5269	Embedded Systems and RTOS	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Identify the functioning of embedded systems for different applications.
CO2	Develop embedded system programming skills.
CO3	Design, implement and test an embedded system.
CO4	Identify the unique characteristics of real-time embedded systems.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1						2
CO2						2
CO3						3
CO4						2

Syllabus:

Introduction to Embedded Computing: Embedded systems Overview, Characteristics ofembedded computing applications, Design Challenges, Common Design Metrics, Processor Technology, IC Technology, Trade-offs.

Process of Embedded System Development: The development process, Requirements, Specification, Architecture Design, Designing Hardware and Software components, system Integration and Testing.

Hardware platforms: Types of Hardware Platforms, Single board computers, PC Add-oncards, custom-built hardware platforms, ARM Processor, CPU performance, CPU power consumption, Bus-based computer systems, Memory devices, I/O devices ,component interfacing, Designing with microprocessors, system level performance analysis.

Program Design and Analysis: components for Embedded programs, Models ofprograms, Assembly, Linking, and loading, basic compilation techniques, software performance optimization ,program level energy and Power analysis, Program validation and Testing.

Real-Time Operating Systems: Architecture of the kernel, Tasks and Task Scheduler,Scheduling algorithms, Interrupt Service Routines, Semaphores, Mutex, Mailboxes, Message queues, Event Registers, Pipes, Signals, Timers, Memory management, Priority Inversion problem. Overview of off-the shelf operating systems-MicroC/OS II, Vxworks, RT Linux.

Overview of Hardware –Software co design

Learning Resources:

Text Books:

1. Wayne Wolf: Computers as Components-Principles of Embedded Computer System Design, Morgan Kaufmann Publisher-2006.

2. David E-Simon: An Embedded software Primer, Pearson Education, 2007.
3. K.V.K.K. Prasad Real-Time Systems: Concepts Design and Programming, Dreamtech Press, 2005.

Course Code: EC5270	Reliability of Devices and Circuits	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Define the reliability of electronic device and circuit
CO2	Understand the failure mechanisms of electronic device and circuit
CO3	Understand the concept of yield in electronic manufacturing
CO4	Resolve the reliability is issues in VLSI design
CO5	Predict the circuit performance using reliability models

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1					1	
CO2					1	
CO3		1				
CO4					2	
CO5	2					2

Syllabus:

Background and Introduction: Definitions of reliability, failure modes, mechanisms, Basic concepts – Reliability functions, Relationship between these functions – Baths tubs curve – Exponential failure density and distribution functions - Expected value and standard deviation of Exponential distribution – Measures of reliability – MTTF, MTTR, MTBF

Introduction to mathematical methods for reliability: Failure rates, Normal distribution function, Six Sigma, Exponential, Weibull and Lognormal distributions for reliability modeling. Manufacturing yields.

Physics of failure based models for : Mass transport-induced failures (electromiration and stress voiding), Electronic charge-induced failures (Dielectric breakdown, Hot carrier effects, Electrical over-stress and Electrostatic discharge), Environmental damage (moisture ingress, corrosion, radiation damage), Degradation of interconnects (solder creep and fatigue).

Circuit Performance considering NBTI, PBTI, oxide breakdown, random telegraph noise, radiation damage, impact of parasitic effects, process temperature variation, Electromagentic compatibility (EMC), Electromagnetic Interference (EMI) and Electrostatic Discharge (ESD).

Introduction to semiconductor device packaging: Materials and processes used for semiconductor device packaging, stresses induced because of packaging.

Learning Resources:

Text Books:

1. M. Ohring, Reliability and Failure of Electronic Materials and Devices, First Edition, Academic Press, 1998.
2. J.W. McPherson, Reliability Physics and Engineering, Second Edition, Springer, 2013.
3. Yuan Taur and T. Ning, “Fundamentals of Modern VLSI Devices,” Cambridge University Press, 1998.
4. J.Ross, Microelectronic Failure Analysis, Sixth Edition, ASTM International, 2011.

Course Code: EC5271	Modern Computer Architecture	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the micro-architectural design of processors.
CO2	Evaluate performance of different architectures with respect to various parameters
CO3	Analyze performance of different ILP techniques
CO4	Identify cache and memory related issues in multi-processors
CO5	Understand the concept of multiscalar architecture

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2			2	3	
CO2	1			2	3	3
CO3	1	2		2	3	3
CO4						
CO5						

Syllabus:

Introduction to high performance computing, RISC philosophy and overview of pipelined

architecture. Performance evaluation of pipelined architecture. Limitations of scalar pipelines, Instruction level parallelism,

Superscalar architecture: Instruction flow optimization, Handling branches, Advanced optimization in instruction flow, register flow techniques: Register renaming and out of order execution.

Advanced data flow techniques: Instruction reuse and value prediction, Memory data flow, Advanced memory data flow architectures, performance evaluation of superscalar architectures.

Multi-threading: Simultaneous multithreaded (SMT) architectures, SMT architecture: Choices,

SMT performance on various designs, SMT architecture: OS impact and adaptive architectures.

Multiscalar architecture: Multi-core Architectures, Multicore Interconnect – NOC, Network-

on-Chip, Cache Coherence, Cache Consistency model, Dynamic Core architectures, GP-GPU Architecture, CPU-GPU Integration.

Learning Resources:

Text Books:

1. J.L. Hennessy, and D.A. Patterson, Computer Architecture: A quantitative approach, Fifth Edition, Morgan Kaufman Publication, 2012

2. J.P. Shen and M.H. Lipasti, Modern Processor Design, MC Graw Hill, Crowfordsville, 2005.

Course Code: EC5272	Organic Electronics	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand "what is organic electronics good for?"
CO2	Learn about structure and properties of organic materials and devices, their functioning and properties, and field of applications
CO3	Explain charge transport, energy levels and doping in organic electronic materials
CO4	Exemplify the optical properties and applications of organic electronic materials, such as in displays and photovoltaic systems
CO5	Exemplify the architecture, characterization, and utilization of electronic components based on organic electronic materials (such as transistors)

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3		1	
CO2	2		2		1	1
CO3	1		3		2	1
CO4	1		2		3	
CO5		2		1	3	

Syllabus:

Introduction to Organic electronics: Overview, history, Common language, crystal structure & binding

Optical properties of organic semiconductors: Born-Oppenheimer approximation & Franck-Condon principle; Transitions between states: Fermi's golden rule; Excitons, Spin, Energy transfer; Exciton diffusion and recombination

Electronic properties of organic semiconductors: Energy bands, electron transport, conduction, mobility, doping, HJs

Materials growth & purification, device patterning, packaging

Light Emitters: basics, efficiency, fluorescence, phosphorescence, TADF, Rolloff, White OLEDs, outcoupling, reliability

Light Detectors: basics, efficiency, architect, materials, transparency, Multijunction OPV, reliability, modules

Transistors: basics, architectures, morphology, reliability, organic transistor circuit applications

Learning Resources:

Text Books:

1. Organic Electronics: Foundations to Applications, Stephen R. Forrest, Oxford University Press, 2020, 1st edition.