✧ Selection and Mode of Payment:

Selected candidates will be intimated through E-Mail. They have to remit the necessary course fee to the Bank as per the details given below.

Outstation participants requiring accommodation and boarding facilities have to pay Rs. 2,000/- in addition to the course fee.

Account Name	GIAN NITW
Account No	**62447453600**
BANK	**State Bank of India**
Branch	**REC Warangal (NIT Campus)**
Branch Code	20149
IFSC Code	SBIN0020149
REC Warangal (NIT Campus)	**506004011**

Candidates registering early will be given preference in short listing process. For any queries regarding registration of the course, please contact the Course Coordinators:

Dr. P. Sreehari Rao
Department of Electronics and Communication Engineering, NIT, Warangal – 506004, Telangana
Tel: +91 8702462439 (O)
+91 9441342324
Email: patri@nitw.ac.in;
patri.srihari@gmail.com

✧ About GIAN Course:

Ministry of Human Resource Development (MHRD), Government of India (GoI) has launched an innovative program titled "Global Initiative of Academic Networks (GIAN)" in higher Education, in order to garner the best international experience. As part of this, internationally renowned Academicians and Scientists are invited to augment the Country's academic resources, accelerate the pace of quality reforms and elevate India's scientific and technological capacity to global excellence.

✧ About the Institute and Warangal:

National Institute of Technology, Warangal (NITW) formerly known as RECW is the first among seventeen RECs set up in 1959. Over the years, the Institute has established itself as a premier Institution in imparting technical education of a very high standard, leading to B.Tech, M.Tech and Ph.D. programmes in various specializations of Science and Engineering streams. Warangal is known for its rich historical and cultural heritage. It is situated at a distance of 140 km from Hyderabad. Warangal is well connected by rail and road. National Institute of Technology, Warangal campus is 3 km away from Kazipet railway station and 12 km away from Warangal railway station.

✧ About the Department

The Department of Electronics and Communication Engineering offers an Undergraduate program in Electronics and communication Engineering and three Postgraduate programs in EI, VLSI, and ACS Specializations. The Department has experienced faculty and well-established laboratories. The Department has liaison with reputed industries and R&D organizations like DRDO, ISRO ECIL, Analog Devices Bangalore and C-DAC.

GIAN GLOBAL INITIATIVE OF ACADEMIC NETWORKS

MHRD Govt. of India सत्यमेव जयते

Five Days GIAN Course on

ADVANCED CMOS CLOCK GENERATION CIRCUITS

December 25th-29th , 2017

Call for Registration and Participation

International Faculty

Dr. Pavan Kumar Hanumolu
Professor, Department of ECE
University of Illinois, Urbana-Champaign

Principal Coordinator
Dr. Sreehari Rao Patri

Co-Cordinator
Sri PMuralidhar

Department of Electronics and Communication Engineering,
National Institute of Technology Warangal
506 004, Telangana, India

Overview of the Course:

Phase-locked loops (PLLs) are de-facto clock generators in digital, analog, and communication systems. They are used to: (i) generate clocks across a wide range of frequencies (MHz to GHz), (ii) clean-up noisy clocks, (iii) perform clock recovery, and (iv) provide frequency/phase modulation. In all these applications, they take up valuable resources in terms of area and power. PLLs have been conventionally implemented using analog architectures such as the charge-pump topology. Because they consume large area and are sensitive to transistor imperfections, more recently they are being realized using mostly digital architectures. However, both analog and digital PLLs suffer from fundamental noise, power, and bandwidth tradeoffs that must be carefully managed. This course seeks to provide the know-how to make these tradeoffs judiciously.

This course entails analysis and design of phase-locked loop (PLL) architectures and circuits. Emphasis will be on fundamental understanding, design intuition, and implementation of PLLs in modern-day CMOS processes. Topics include charge-pump phase-locked loops, noise properties of PLLs, integer/fractional-N PLLs, digital PLLs, delay-locked loops, and injection-locked clock multipliers. Supply noise mitigation techniques will be covered in detail.

Course Objectives:

The primary objectives of the course are as follows:

- Understanding of basic and advanced PLL architectures
- Modelling of PLLs
- Exposure to circuit design of building blocks
- Provide design intuition
- Identification and mitigation of the impact of supply noise
- Exposure to practical problems of PLL's and their solutions, through case studies.

International Faculty:

Dr Pavankumar Hanumolu is a Professor at the Department of ECE, University of Illinois, Urbana-Champaign. Prof Hanumolu's research and teaching experience spanned over several years. Before this position, Dr Hanumolu was faculty of school of EECS, Oregon State University, Corvallis, OR USA for 7 years. He authored over 60 peer-reviewed publications in IEEE Journal on solid state circuits and IEEE transactions circuits and systems and 80 IEEE international conference papers. Prof. Hanumolu is the recipient of the Dean's Award for Excellence in Research for the year 2017. Dr. Hanumolu received the National Science Foundation CAREER Award in 2010, the Engelbrecht Young Faculty Award in 2009, the Professor of the Year Award in 2008, and the Faculty of the Year Award in 2011 from the College of Engineering and the School of EECS at Oregon State University. He was a co-recipient of the Custom Integrated Circuits Conference (CICC) 2006 best student paper award. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS from 2008 to 2010 and a Guest Editor of the Journal of Solid-State Circuits from 2009 to 2011. He currently serves as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, as a member of the IEEE Custom Integrated Circuits Conference and VLSI Circuits Symposium Technical Program Committees.His research pursuits are at the intersection of device physics and fabrication technology, microarchitecture, power electronics, and systems (signal processing, communications and control). Prof. Hanumolu's research builds upon his stellar reputation in high-speed serial links, expanding into two new areas: energy proportional high-speed serial links and time-based analog circuits. His group developed novel circuit and system design techniques to enable high-speed serial links to achieve close to zero quiescent power when idle, while achieving rapid start-up in the range of 10s of nanoseconds when required to transmit. His group engineered techniques to represent information in terms of signal phase using a voltage controlled oscillator (VCO) and developed efficient techniques to process it. His contributions in this area include the design of time-based analog-to-digital converters, continuous time-filters, and high switching frequency DC-DC converters...

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Who can participate?

This program is open to the Faculty, Post graduate students, Engineers from industry , Research Scholars working in the relevant areas and scientists at R&D laboratories..

How to Register?

Stage-1: Web Portal Registration:
Visit http://www.gian.iitkgp.ac.in/GREGN/index and create login User ID and Password. Fill up the blank registration form and do web registration by paying Rs. 500/- online through Net Banking / Debit / Credit card. This provides the user with life time registration to enrol in any number of GIAN courses offered.

Stage-2: Course Registration:
Login to the GIAN portal with the user ID and Password already created in Step 1. Click on Course Registration option at the top of Registration Form. Select the Course titled "**ADVANCED CMOS CLOCK GENERATION CIRCUITS"**" from the list and click on Save option. Confirm your registration by clicking on Confirm Course.

Registration Fee:

Faculty	**Rs. 2,000/-**
Participants from Industry / Research organizations	**Rs. 4,000/-**
Students & Scholars Without award of grade With award of Grade	 Rs 500/- Rs 1,000/-
Participants from abroad	**US $ 200**

The Registration fee includes instructional materials, laboratory use and session teas.

The out-station participants will be provided with boarding and lodging on additional payment of Rs. 2,000/- in Student Hostel on sharing basis